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# MS-7366 Micro ATX

Version: 2.1\_071030C

**CPU:** Intel Pentium 4 Cedar Mill / Prescott , Pentium D Smithfield / Presler and Conroe / Kentsfield family processors in LGA775 Package.

## System Chipset:

**NVIDIA MCP73**

## On Board Device:

**BIOS -- SPI Flash 8M**  
**Azalia Codec -- ALC888**  
**LPC Super I/O -- FINTEK F71882FG**  
**LAN -- Realtek RTL8211BL-GR**  
**CLOCK Gen -- Integrated in MCP73**  
**1394 Controller -- JMB381**

## Main Memory:

**Dual-channel DDR-II \* 2 (Max 4GB)**

## Expansion Slots:

**PCI EXPRESS X16 SLOT \*1**  
**PCI EXPRESS X1 SLOT \* 1**  
**PCI SLOT \* 2**

## Intersil PWM:

**Controller: ST L6703 (3 Phases)**  
**Driver:ST L6703**

OPT	Function	Orcad Configure	BOM
A	MCP73U(HDMI,D-SUB)/F71882FG/ALC888/RTL8211BL/JMB381	Cfg-U	601-7366-B10
B	MCP73PV(DVI,D-SUB)/F71882FG/ALC888/RTL8211BL	Cfg-PV	601-7366-B20
C	MCP73S(D-SUB)/F71882FG/ALC888/RTL8211BL	Cfg-S	
D	MCP73V(D-SUB)/F71882FG/ALC888/RTL8211CL	Cfg-V	601-7366-B30
E	MCP73U(HDMI,D-SUB)/F71882FG/ALC888/RTL8211BL/JMB381	Cfg-M1	601-7366-06S
*F	MCP73D /F71882FG/ALC888/RTL8211BL/JMB381	Cfg-D	

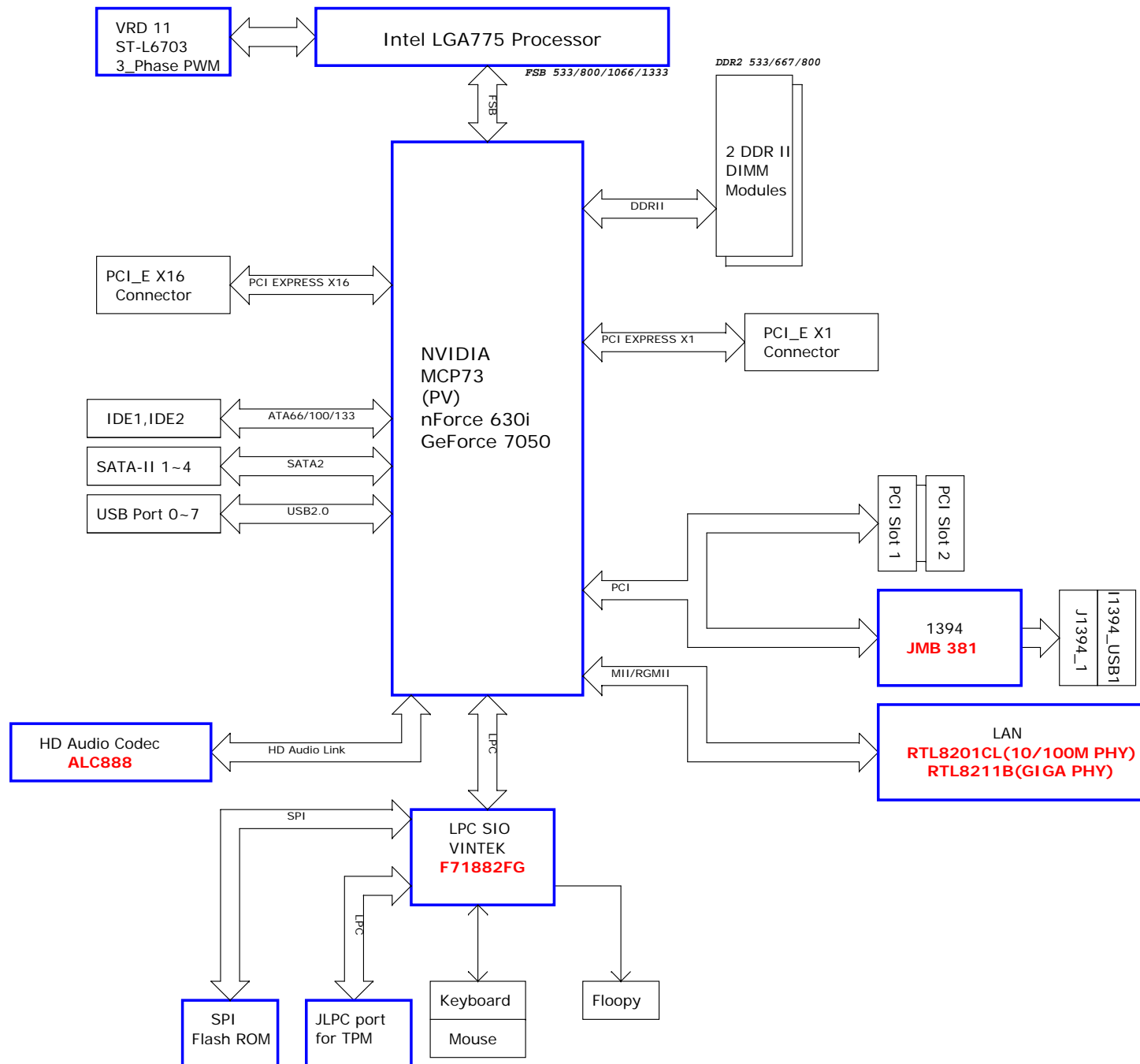


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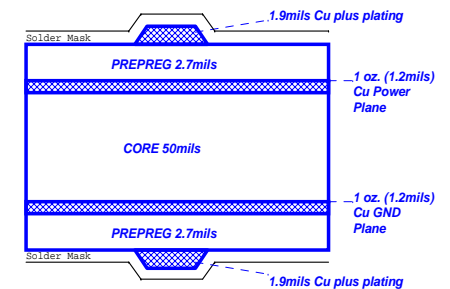
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# Block Diagram



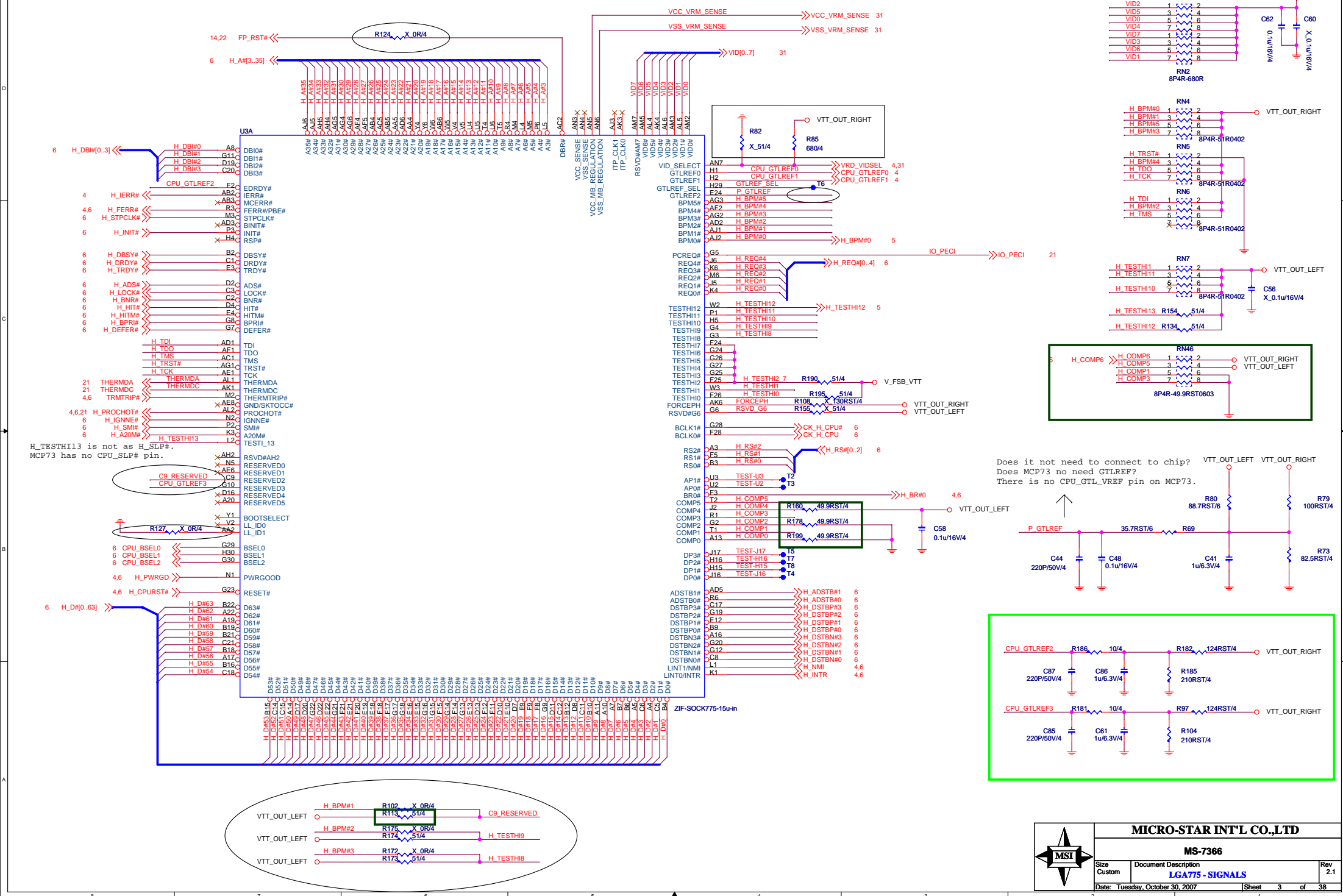
## Board Stack-up

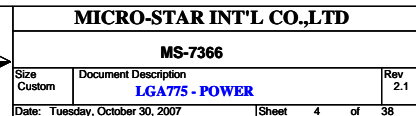
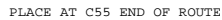
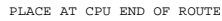
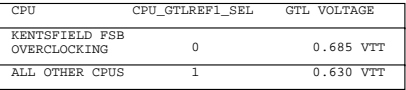
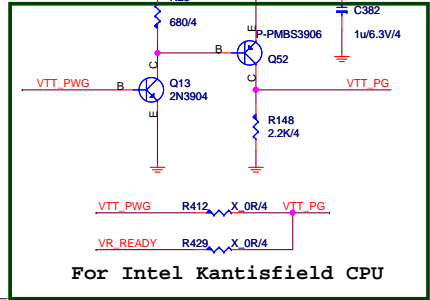
(1080 Prepreg Considerations)



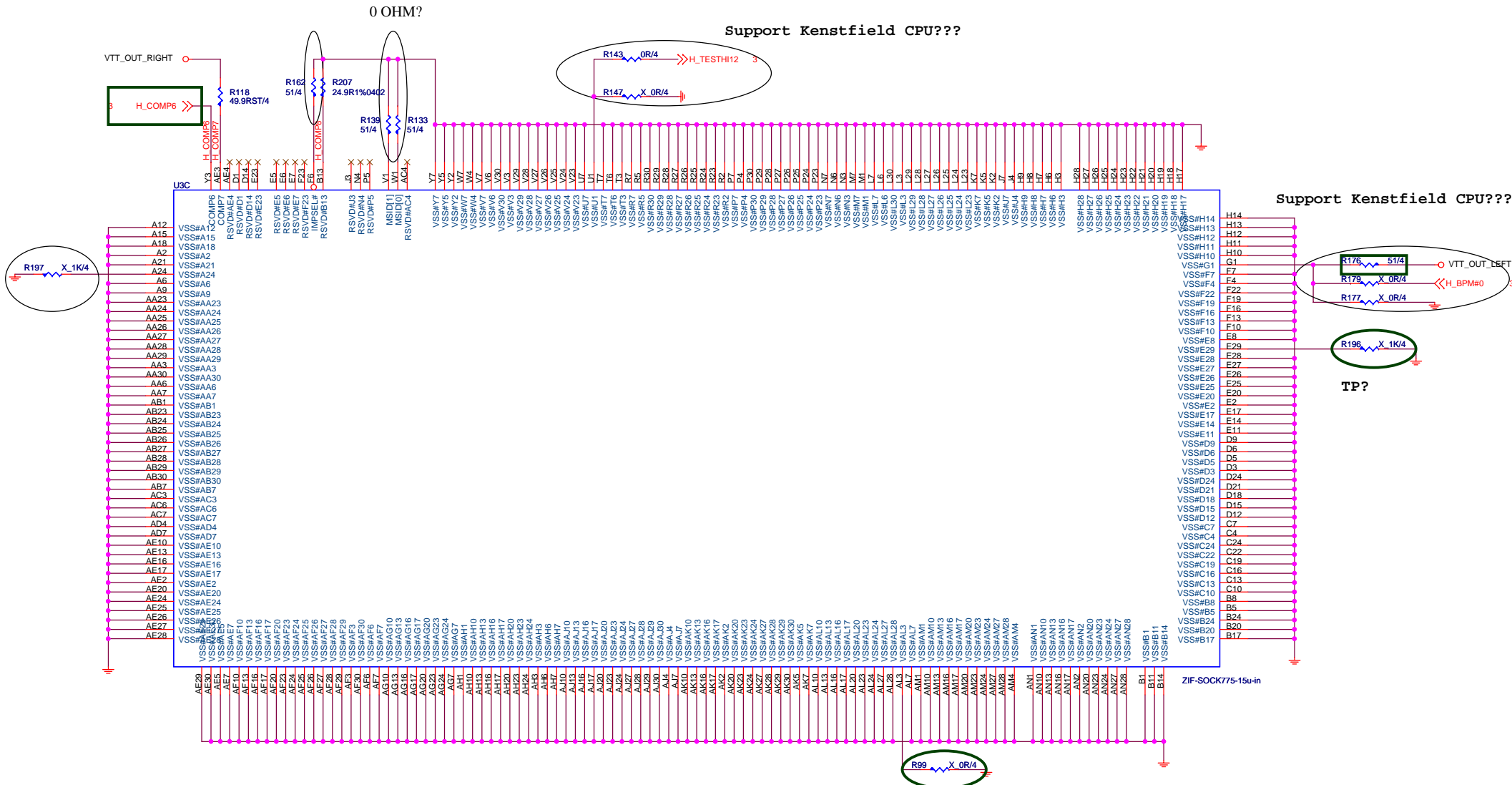
Single End 50ohm Top/Bottom : 4mils  
 USB2.0 - 100ohm : 20/4/8/4/20  
 HDMI - 100ohm : 20/4/8/4/20  
 SATA - 100ohm : 20/4/8/4/20  
 LAN - 100ohm : 20/4/8/4/20  
 PCIE - 100ohm : 20/4/8/4/20  
 IEEE1394 - 110ohm : 15/4/9/4/15  
 IDE : 15/4/8/4/15

### CPU SIGNAL BLOCK

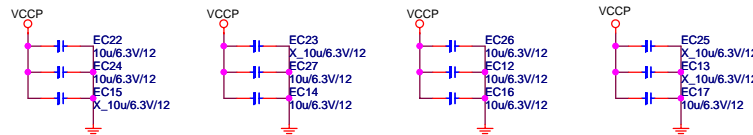




VID_SELECT	VTT_PWG	power on sequence
0 (VRM10)	VID_GD	VTT_PWG before VCCP
1 (VRM11)	VR_READY	VCCP before VTT_PWG



**CPU DECOUPLING CAPACITORS**



Place these caps within socket cavity

3 H\_DBIN[0..3] >> H\_DBIN[0..3]

3 H\_DSTBP#0 >> V36  
3 H\_DSTBN#0 >> W36  
H\_DBIN#0 W37  
3 H\_DSTBP#1 >> N31  
3 H\_DSTBN#1 >> P30  
H\_DBIN#1 R34  
3 H\_DSTBP#2 >> G33  
3 H\_DSTBN#2 >> G35  
H\_DBIN#2 H31  
3 H\_DSTBP#3 >> M38  
3 H\_DSTBN#3 >> N36  
H\_DBIN#3 J35

3 H\_A#[3..35] >> H\_A#3 W34  
H\_A#4 AA34  
H\_A#5 W31  
H\_A#6 W33  
H\_A#7 W32  
H\_A#8 AA32  
H\_A#9 AA31  
H\_A#10 AB30  
H\_A#11 AA30  
H\_A#12 AC35  
H\_A#13 AC34  
H\_A#14 AC33  
H\_A#15 AC32  
H\_A#16 AC31  
H\_A#17 AE30  
H\_A#18 AC30  
H\_A#19 AE34  
H\_A#20 AE33  
H\_A#21 AE31  
H\_A#22 AG33  
H\_A#23 AE32  
H\_A#24 AG35  
H\_A#25 AG34  
H\_A#26 AF30  
H\_A#27 AG31  
H\_A#28 AG30  
H\_A#29 AJ32  
H\_A#30 AJ34  
H\_A#31 AJ33  
H\_A#32 AJ30  
H\_A#33 AJ31  
H\_A#34 AL35  
H\_A#35 AK30

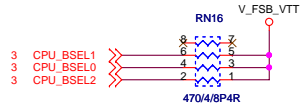
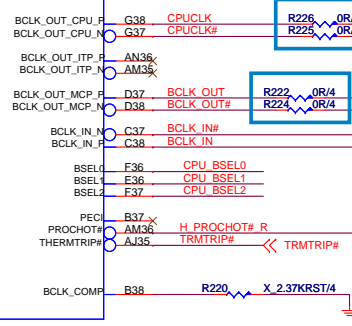
3 H\_ADSTB#0 >> AA33  
3 H\_ADSTB#1 >> AG32  
3 H\_REQ# [0..4] >> H\_REQ#0 V30  
H\_REQ#1 U31  
H\_REQ#2 W30  
H\_REQ#3 W35  
H\_REQ#4 U30

3 H\_ADS# >> AF37  
3 H\_BNR# >> AF36  
3,4 H\_BR#0 >> AH37  
3 H\_BPR# >> AC36  
3 H\_DBSY# >> AE35  
3 H\_DEFER# >> AC37  
3 H\_DRDY# >> AG36  
3 H\_HIT# >> AG38  
3 H\_HITM# >> AG37  
3 H\_LOCK# >> AE36  
3 H\_TRDY# >> AG38  
3 H\_RS# [0..2] >> H\_RS#0 AD36  
H\_RS#1 AD37  
H\_RS#2 AD35

3,4 H\_FERR# >> H\_FERR# AL38  
3 H\_A20M# >> H\_A20M# AH38  
3 H\_IGNNE# >> H\_IGNNE# AK36  
3 H\_INIT# >> H\_INIT# AL36  
3 H\_SMI# >> H\_SMI# AL37  
3 H\_INTR# >> H\_INTR# AH36  
3,4 H\_NMI# >> H\_NMI# AH35  
3 H\_STPCLK# >> H\_STPCLK# AJ36  
3,4 H\_PWRGD >> H\_PWRGD AK37

VTT\_OUT\_RIGHT >> R228 49.9RST/4 AM38  
R231 49.9RST/4 AM37  
CPU\_COMP\_VCC  
CPU\_COMP\_GND

U8A  
7  
SEC 1 OF 10  
MCP73  
CPU\_D0# AB36 H\_D#0  
CPU\_D1# AA36 H\_D#1  
CPU\_D2# AB37 H\_D#2  
CPU\_D3# Y36 H\_D#3  
CPU\_D4# AA35 H\_D#4  
CPU\_D5# Y35 H\_D#5  
CPU\_D6# Y37 H\_D#6  
CPU\_D7# Y38 H\_D#7  
CPU\_D8# U35 H\_D#8  
CPU\_D9# T35 H\_D#9  
CPU\_D10# U36 H\_D#10  
CPU\_D11# T36 H\_D#11  
CPU\_D12# V37 H\_D#12  
CPU\_D13# T37 H\_D#13  
CPU\_D14# R37 H\_D#14  
CPU\_D15# T38 H\_D#15  
CPU\_D16# R31 H\_D#16  
CPU\_D17# U33 H\_D#17  
CPU\_D18# U34 H\_D#18  
CPU\_D19# R30 H\_D#19  
CPU\_D20# U32 H\_D#20  
CPU\_D21# R32 H\_D#21  
CPU\_D22# R33 H\_D#22  
CPU\_D23# R35 H\_D#23  
CPU\_D24# N30 H\_D#24  
CPU\_D25# N32 H\_D#25  
CPU\_D26# N33 H\_D#26  
CPU\_D27# N34 H\_D#27  
CPU\_D28# L30 H\_D#28  
CPU\_D29# L31 H\_D#29  
CPU\_D30# L33 H\_D#30  
CPU\_D31# L32 H\_D#31  
CPU\_D32# L35 H\_D#32  
CPU\_D33# L34 H\_D#33  
CPU\_D34# K30 H\_D#34  
CPU\_D35# J34 H\_D#35  
CPU\_D36# J31 H\_D#36  
CPU\_D37# J30 H\_D#37  
CPU\_D38# J33 H\_D#38  
CPU\_D39# J32 H\_D#39  
CPU\_D40# G31 H\_D#40  
CPU\_D41# G34 H\_D#41  
CPU\_D42# G36 H\_D#42  
CPU\_D43# F33 H\_D#43  
CPU\_D44# E33 H\_D#44  
CPU\_D45# E35 H\_D#45  
CPU\_D46# D35 H\_D#46  
CPU\_D47# D36 H\_D#47  
CPU\_D48# J36 H\_D#48  
CPU\_D49# M37 H\_D#49  
CPU\_D50# R36 H\_D#50  
CPU\_D51# N35 H\_D#51  
CPU\_D52# P37 H\_D#52  
CPU\_D53# P36 H\_D#53  
CPU\_D54# L36 H\_D#54  
CPU\_D55# M35 H\_D#55  
CPU\_D56# M36 H\_D#56  
CPU\_D57# L37 H\_D#57  
CPU\_D58# H36 H\_D#58  
CPU\_D59# H35 H\_D#59  
CPU\_D60# K36 H\_D#60  
CPU\_D61# K37 H\_D#61  
CPU\_D62# H38 H\_D#62  
CPU\_D63# H37 H\_D#63  
CPU\_RESET# C36 >> H\_CPURST# 3,4  
BCLK\_OUT\_CPU\_F >> G38 CPUCLK  
BCLK\_OUT\_CPU\_N >> G37 CPUCLK#  
BCLK\_OUT\_ITP\_F >> AN36  
BCLK\_OUT\_ITP\_N >> AM35  
BCLK\_OUT\_MCP\_F >> D37 BCLK OUT  
BCLK\_OUT\_MCP\_N >> D38 BCLK OUT#  
BCLK\_IN\_N >> C37 BCLK IN#  
BCLK\_IN\_F >> C38 BCLK IN  
BSEL# F36 CPU\_BSEL0  
BSEL# E36 CPU\_BSEL1  
BSEL# F37 CPU\_BSEL2  
PECL >> B37 X  
PROCHOT# >> AM36 H\_PROCHOT# R  
THERMTRIP# >> AJ35 TRMTRIP# 3,4  
BCLK\_COMP >> B38 R220 X 2.37KRST/4



BSEL[2..0]	FSB CLK (MHz)
000	266MHz
001	133MHz
010	200MHz
100	333MHz
TBD	Reserved

Check this pin for CPU function.

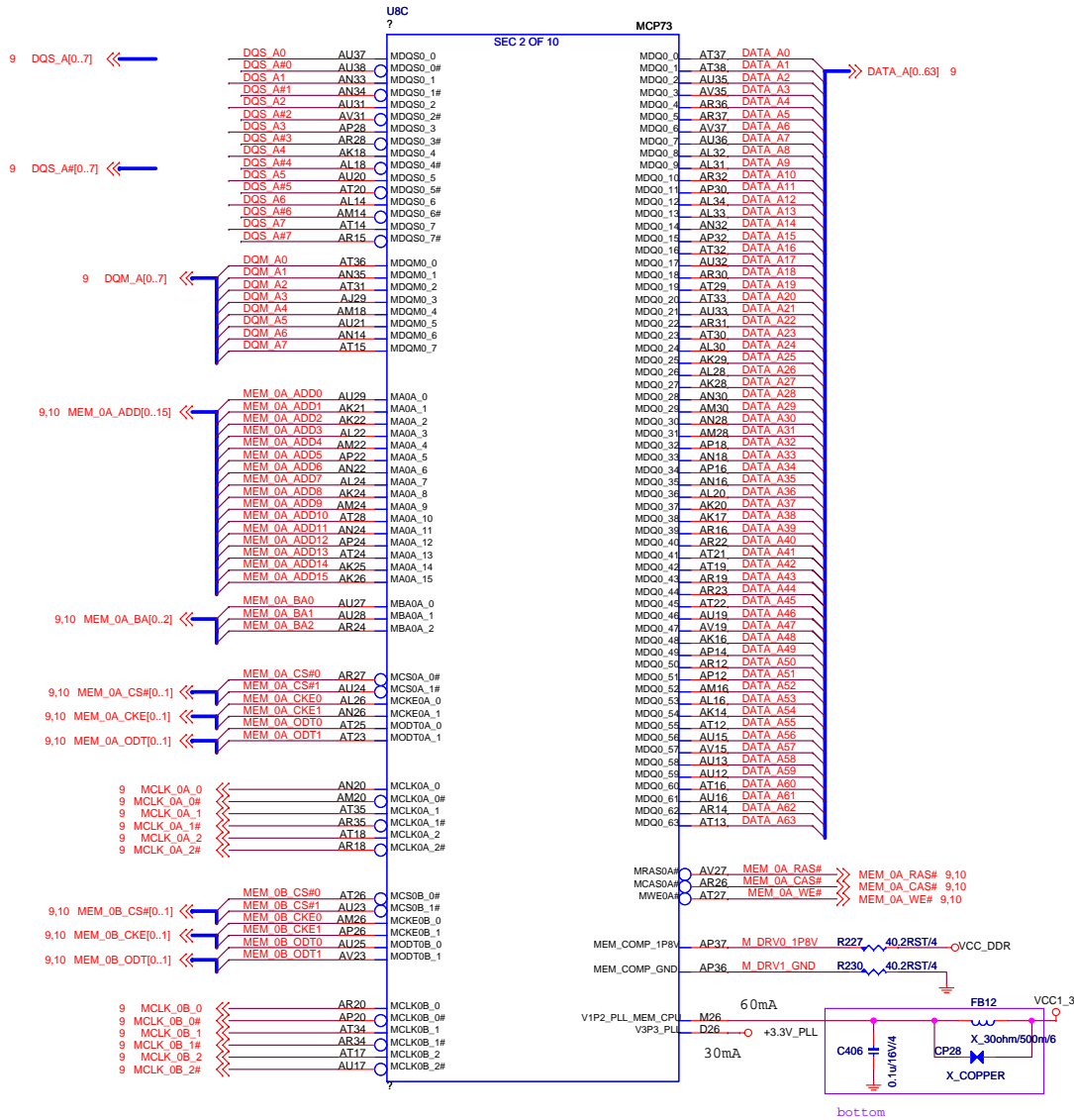


DATA 0

DIMM 1 ADDR 0A / CNTL 0A

DIMM 2 ADDR 0B / CNTL 0B

## DIMM 0A



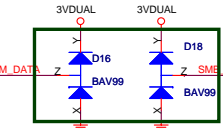
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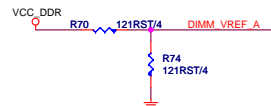
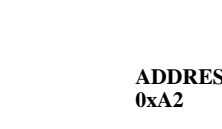
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**DIMM1 / 0A**



**ADDRESS: 0000xA0**

**DIMM2 / 0B**

**ADDRESS: 0010xA2**

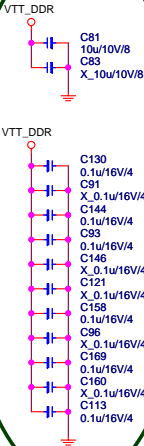


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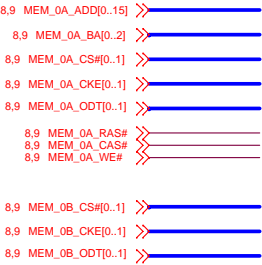
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Size Custom	Document Description <b>DDR II - DIMM 1 &amp; 2 Sockets</b>	Rev 2.1
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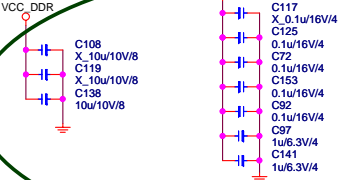
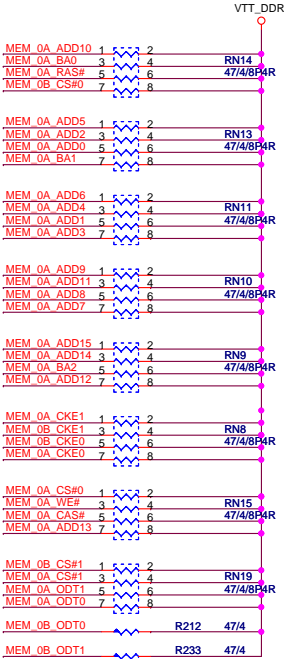
CHANNEL A VTT\_DDR DECOUPLING CAPS



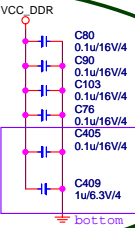
CHECK CAP



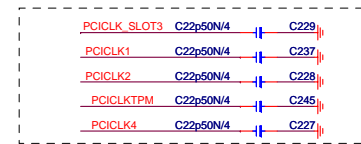
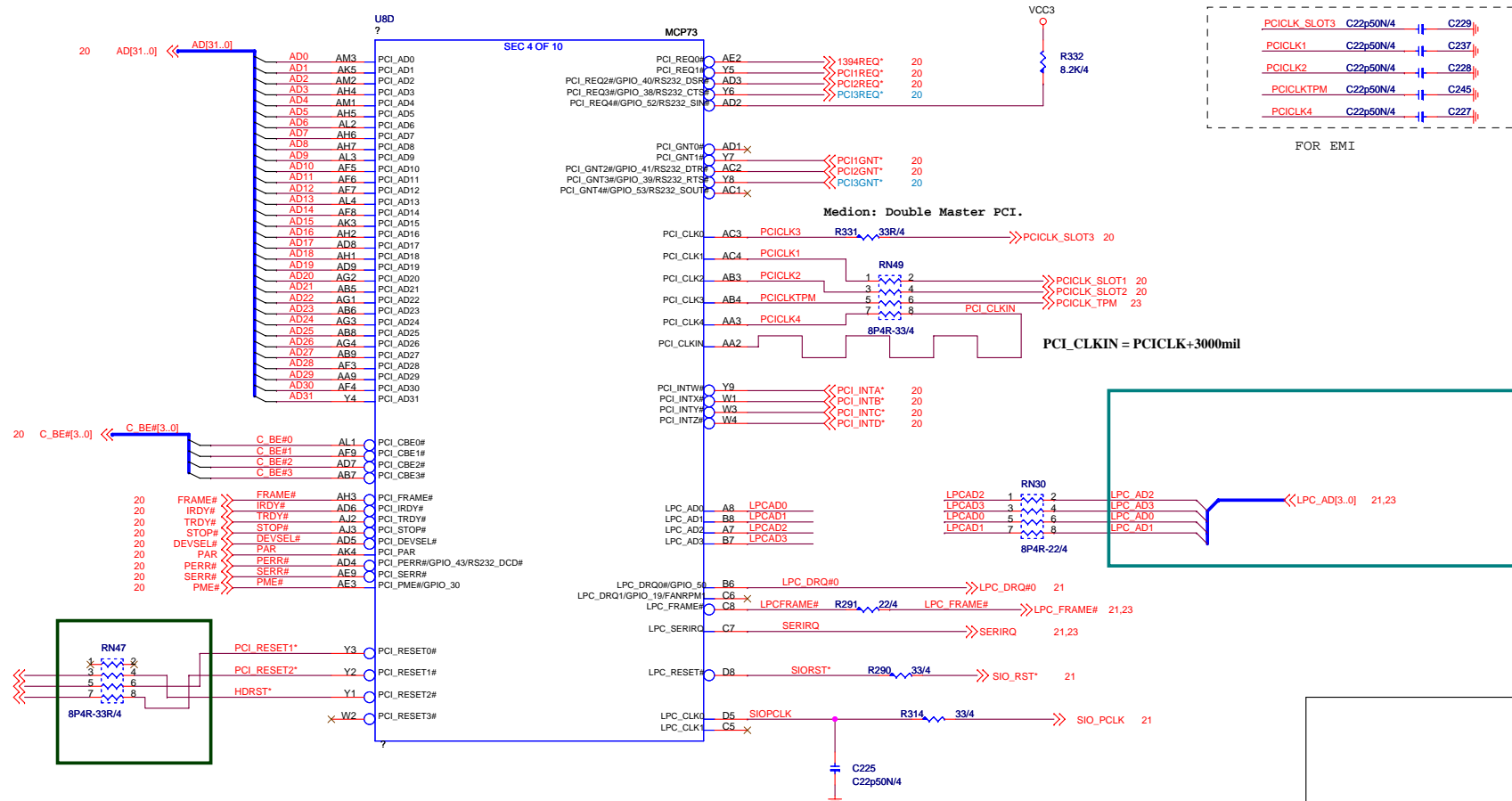
CHANNEL A ----- 0A , 0B



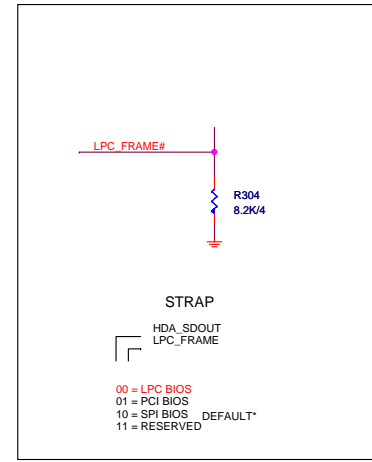
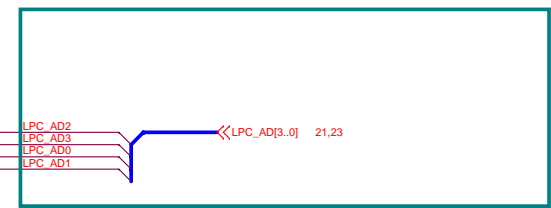
CHECK CAP



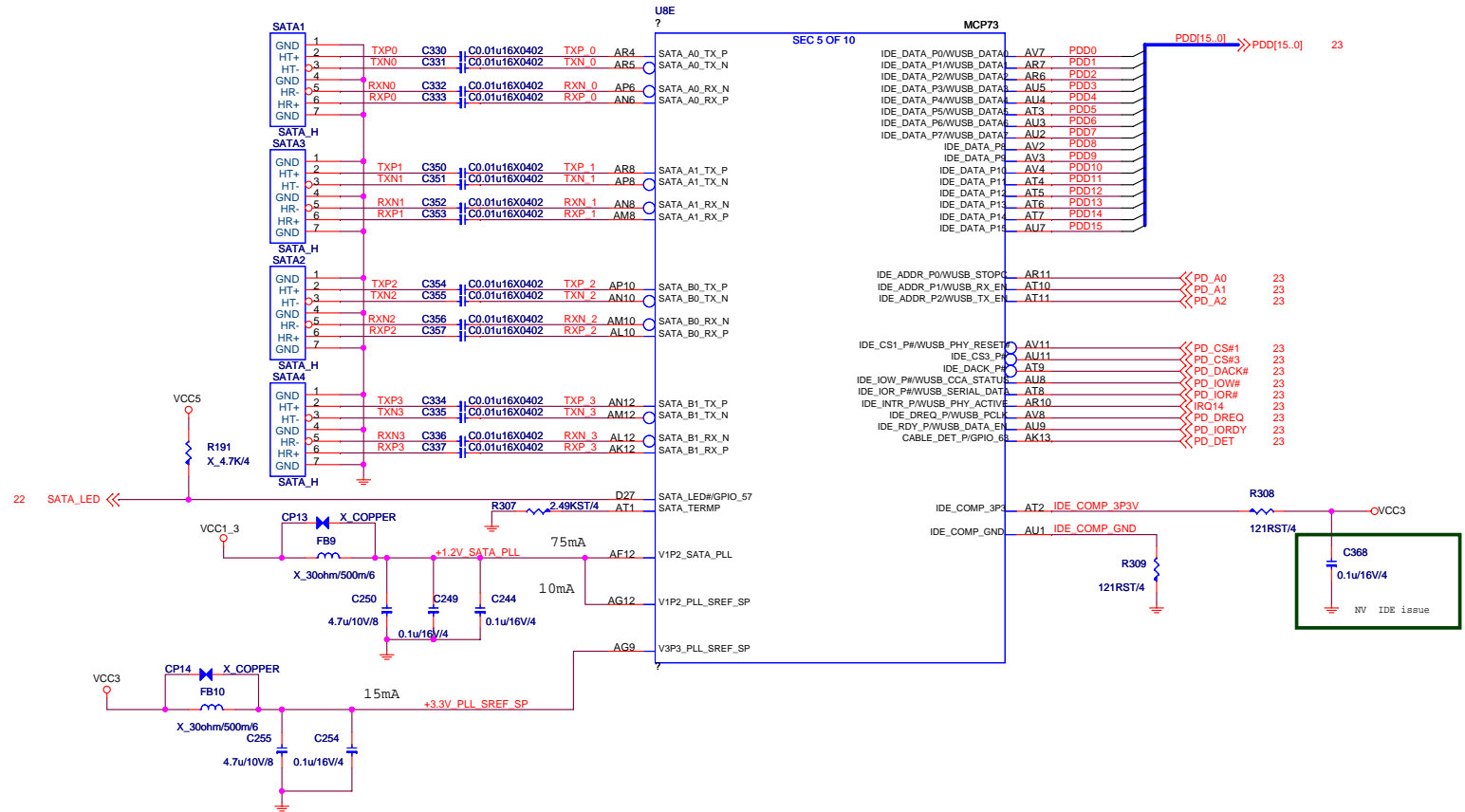
公板上0.1u X5, 1uX3, 10uX3  
兩根再X2



FOR EMI



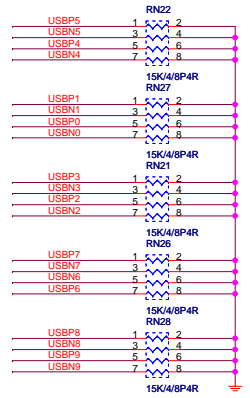
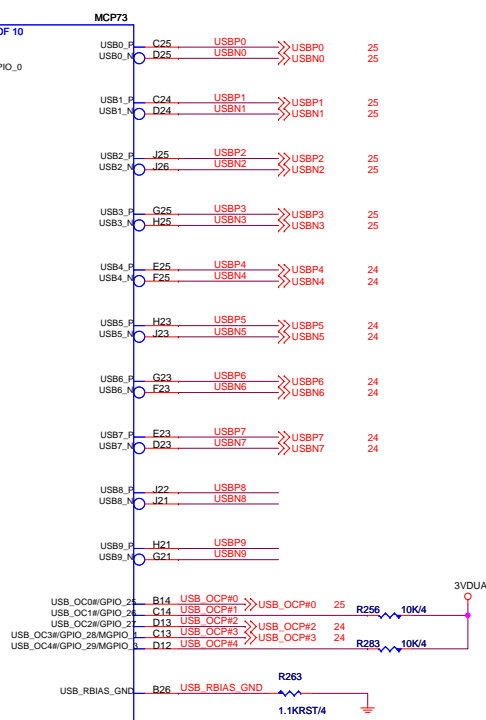
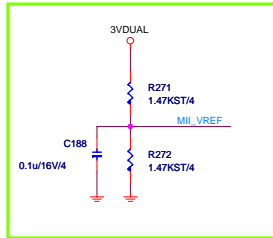
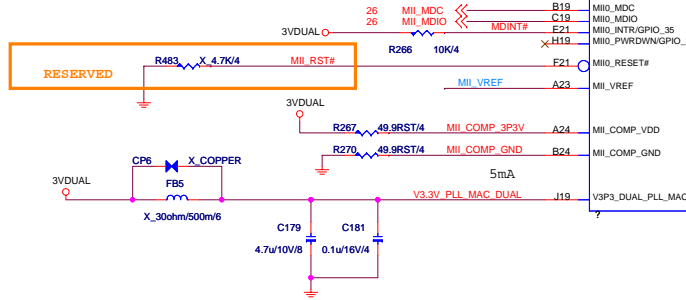
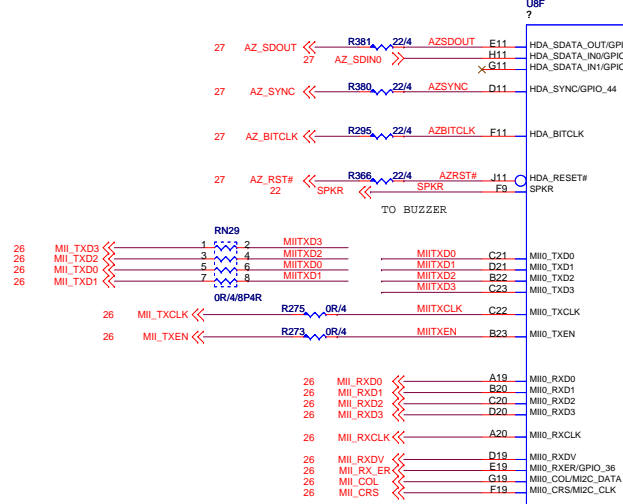
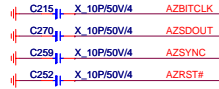
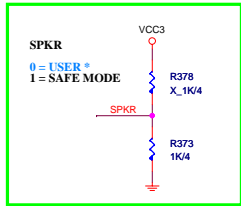
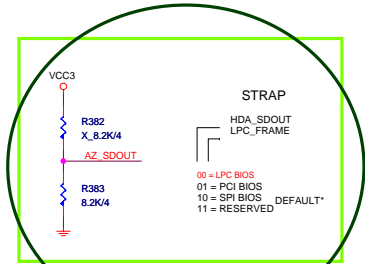
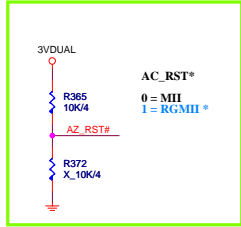
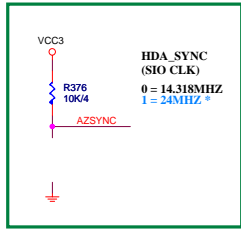
PLACE CAPS AT CONNECTOR.

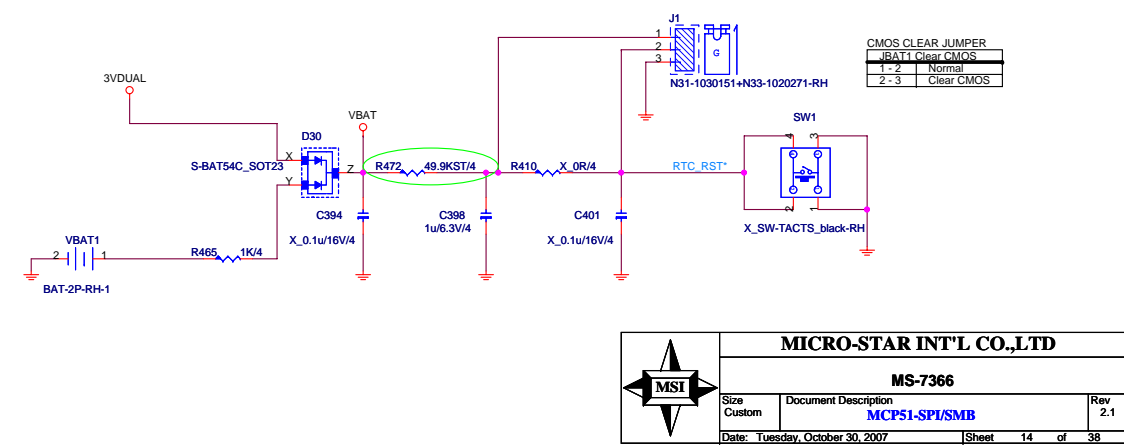
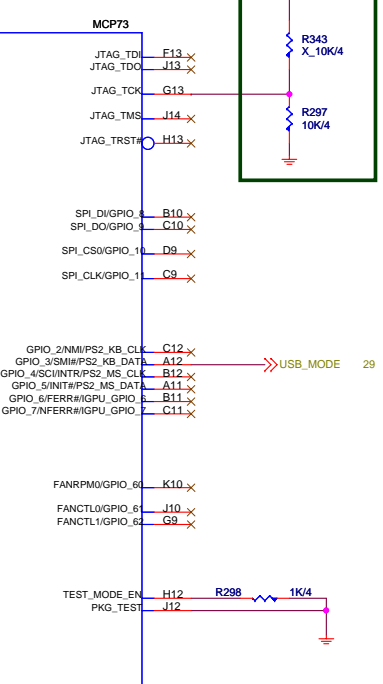
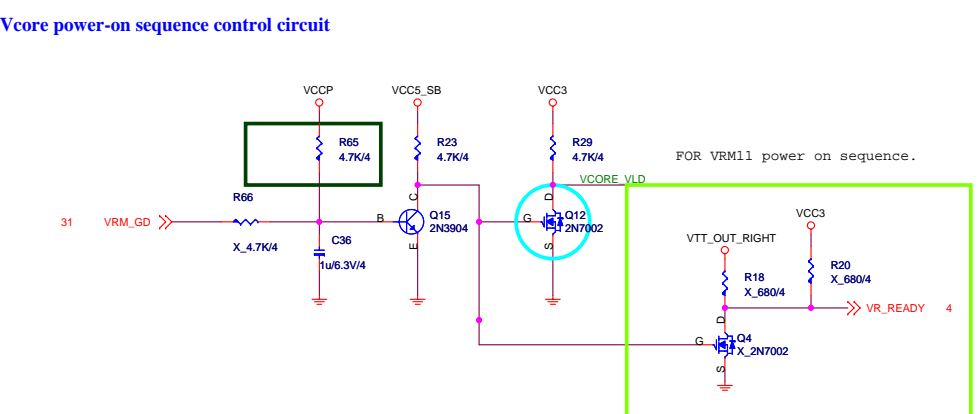
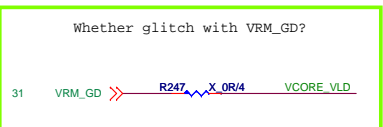
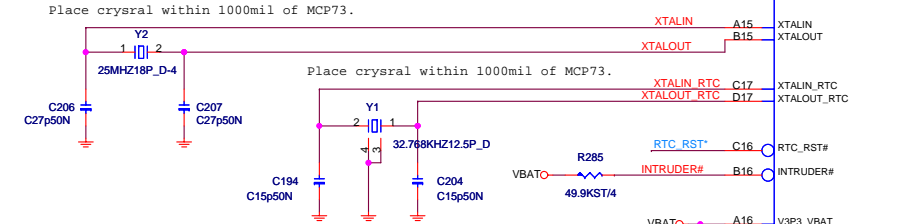
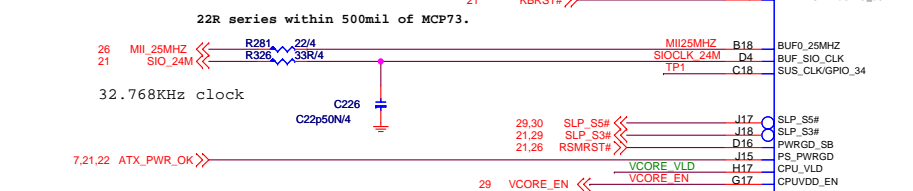
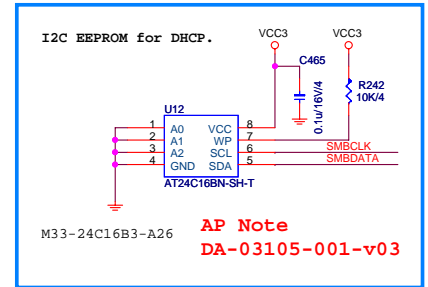
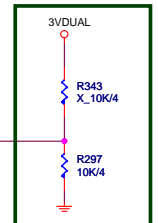
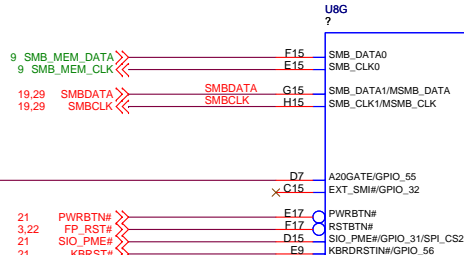
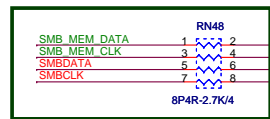


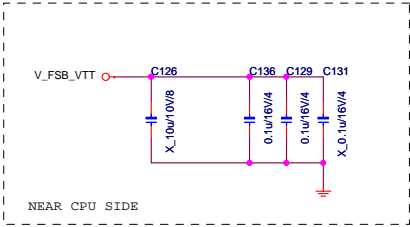
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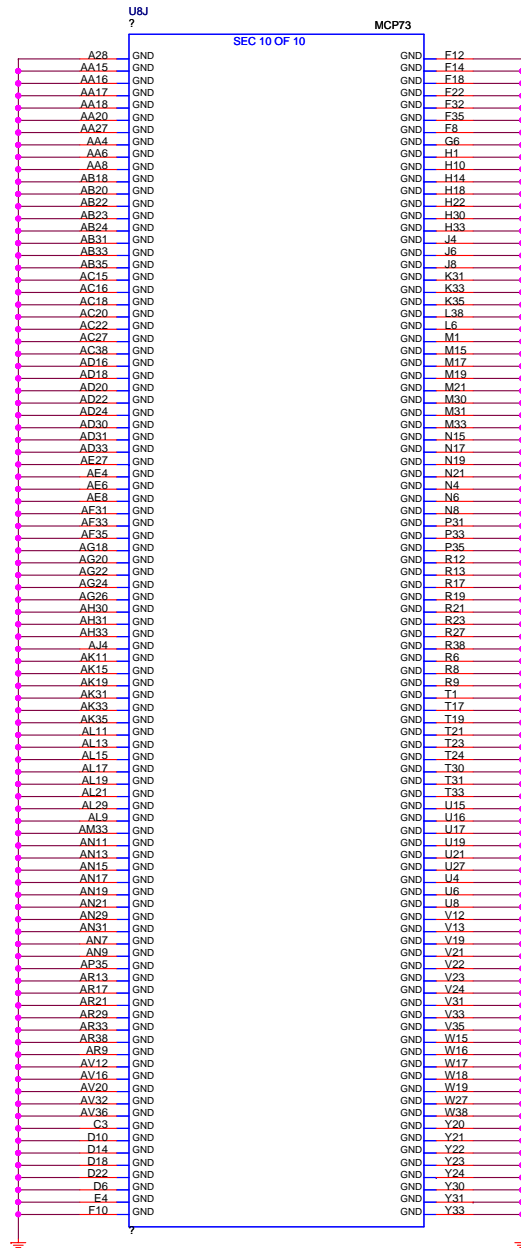
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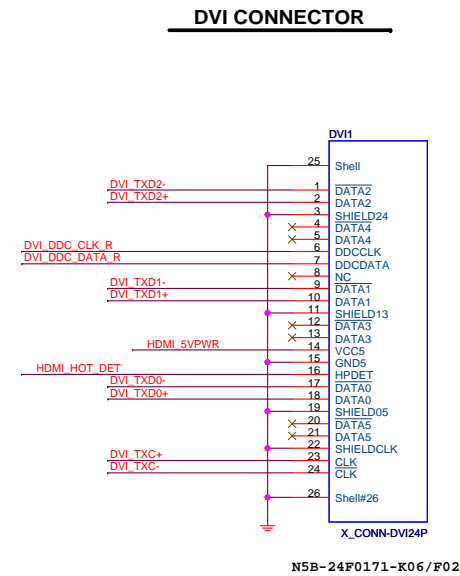
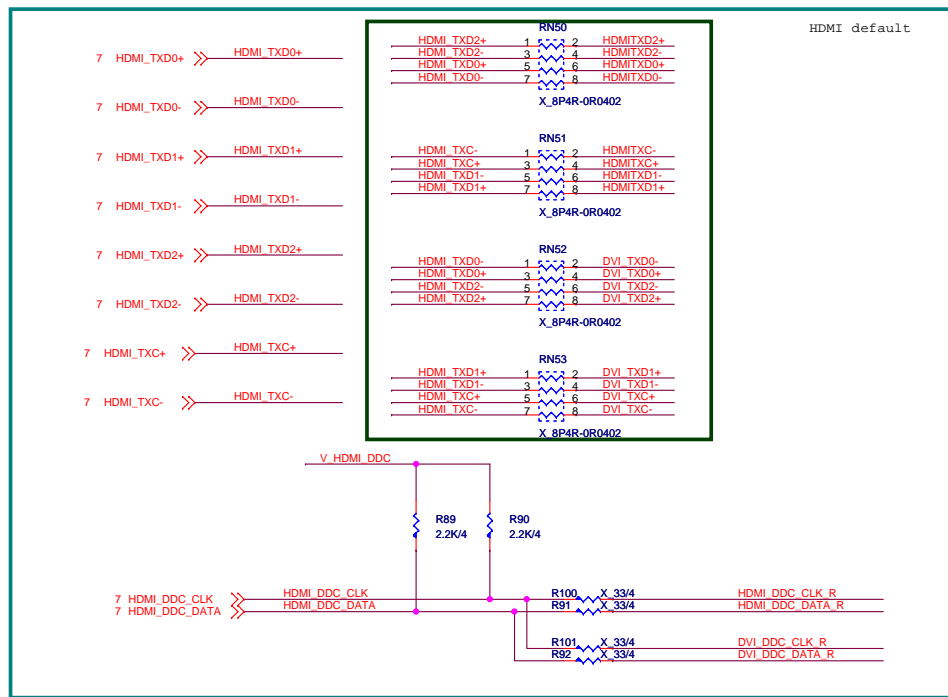
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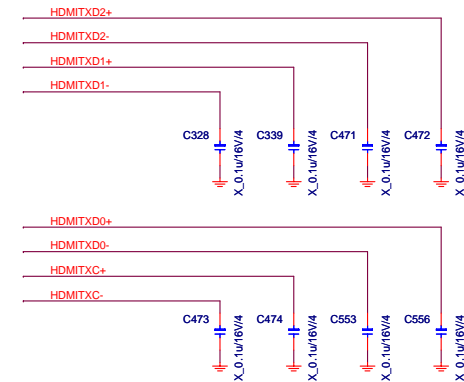
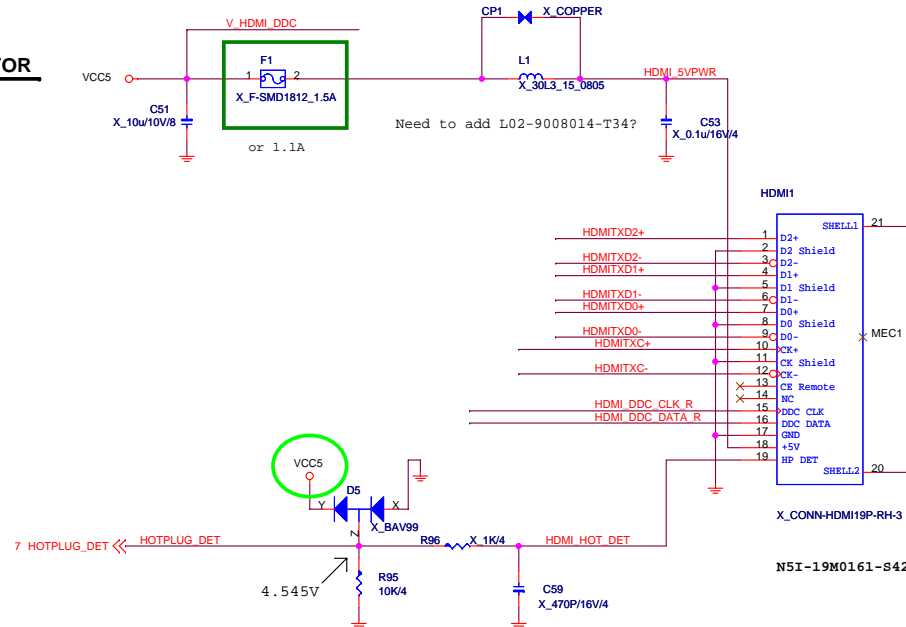
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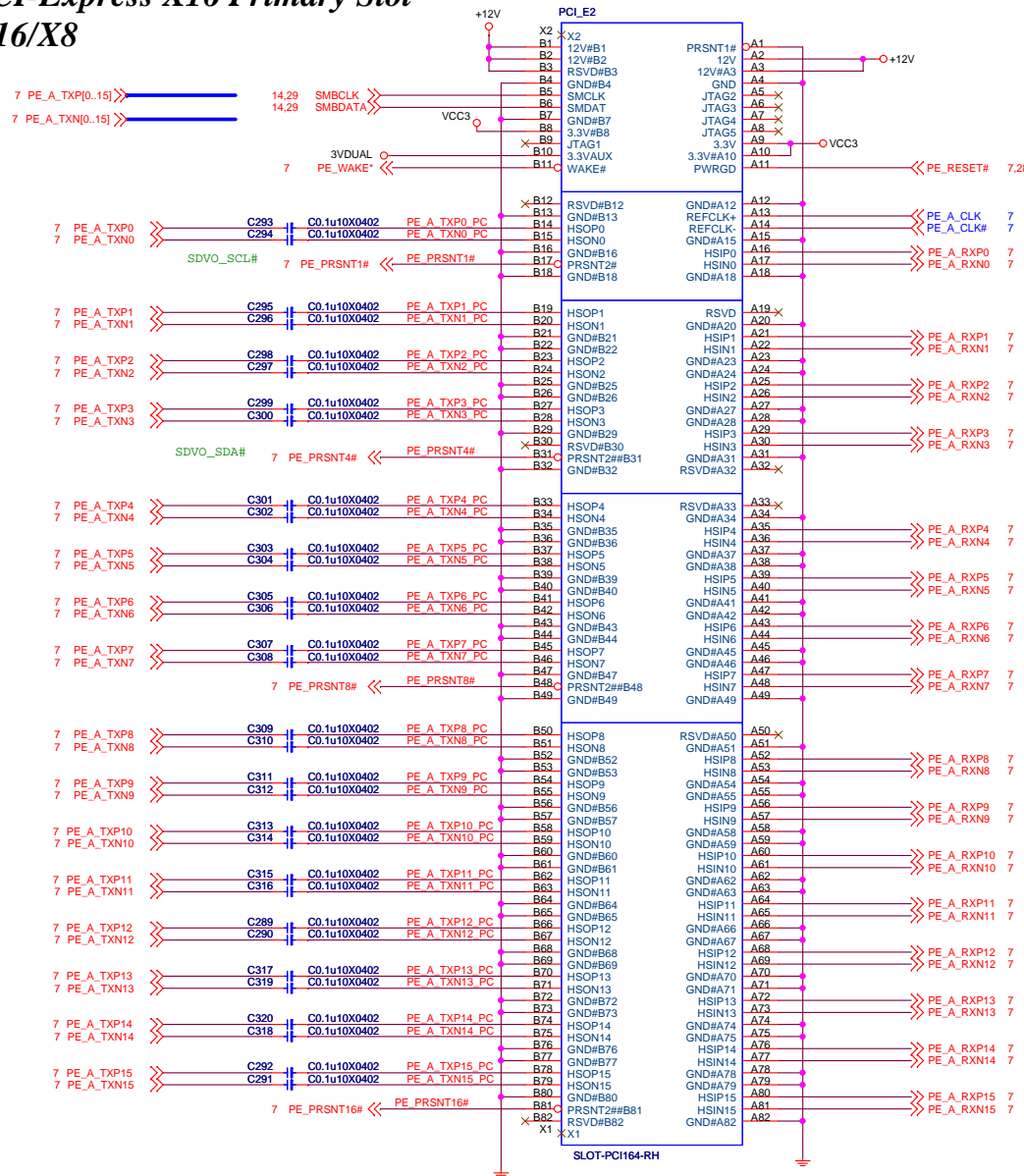




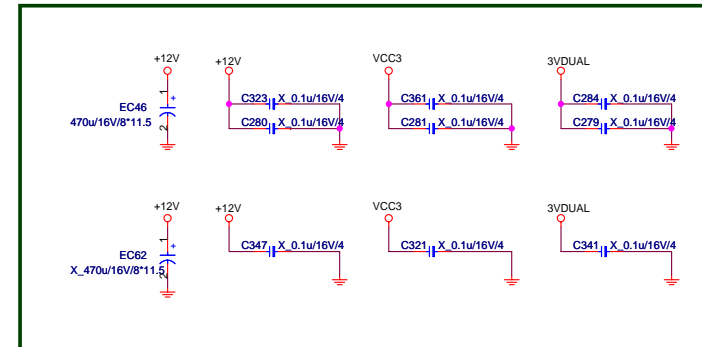
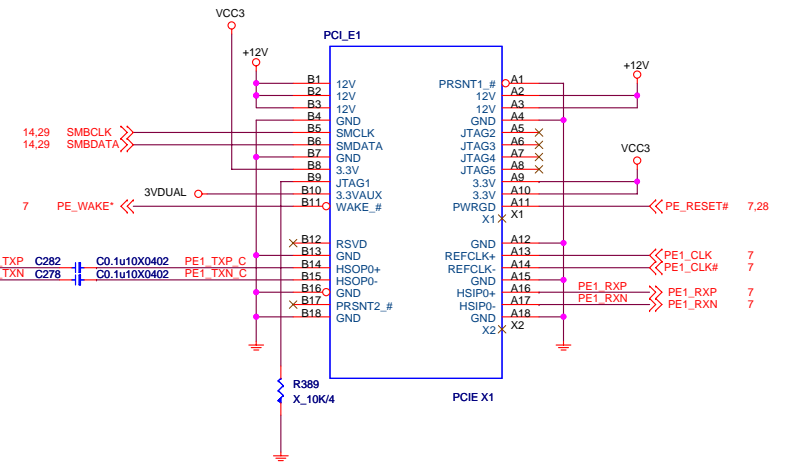
## HDMI CONNECTOR



**PCI-Express X16 Primary Slot**  
**X16/X8**



**PCI-Express x1 SLOT 1**



**MICRO-STAR INT'L CO.,LTD**

MS-7366

Size	Custom
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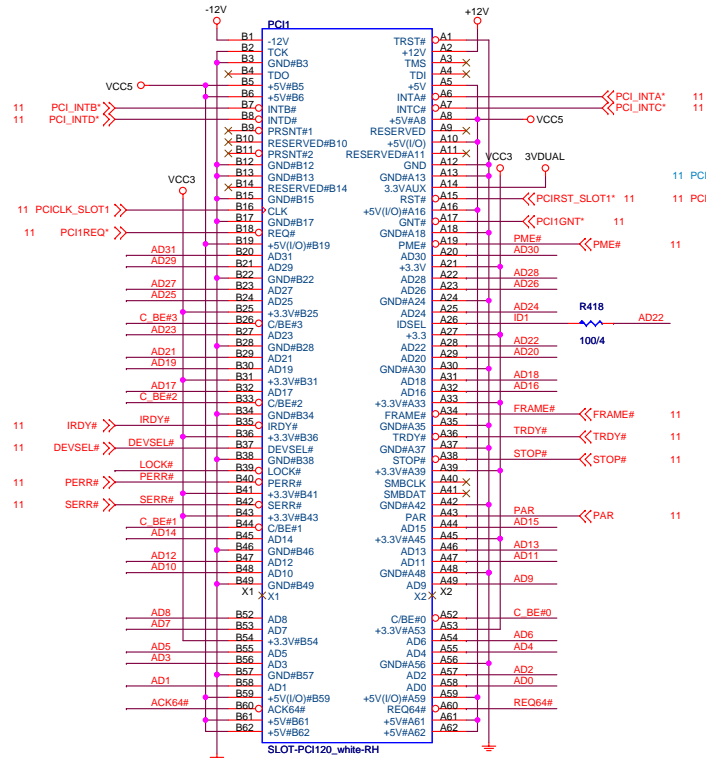
Document Description
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**PCI-E X16/X1 Slot**

Rev	
2.1	

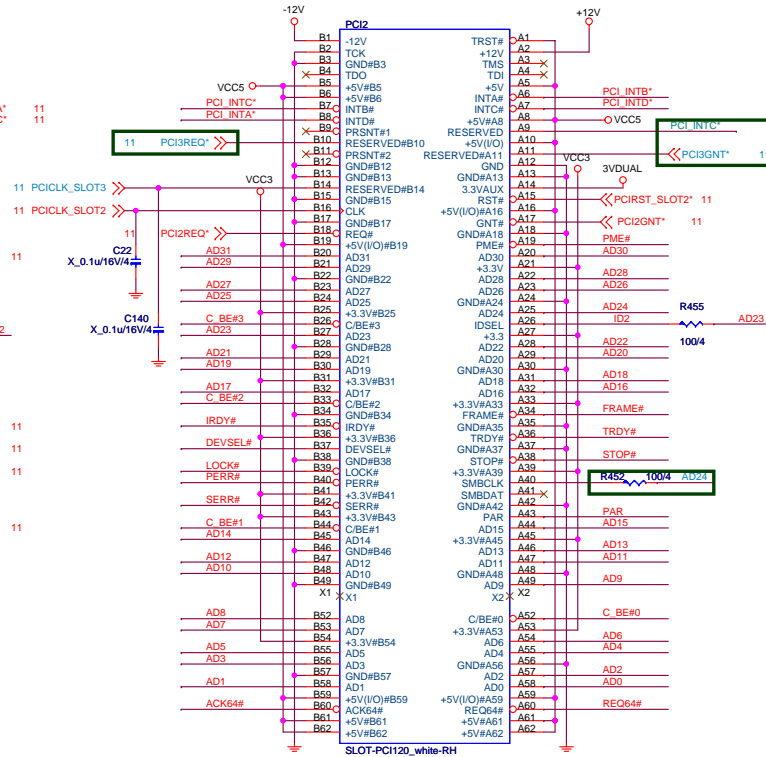
Date: Tuesday, October 30, 2007	Sheet 19 of 38
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# PCI SLOT 1 (PCI VER: 2.2 COMPLY)



IDSEL = AD22  
MASTER = PCI1REQ\*  
PCI1GNT\*  
PCI1ROUTE=A,B,C,D

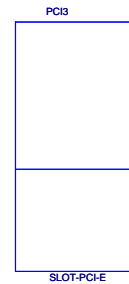
# PCI SLOT 2 (PCI VER: 2.2 COMPLY)



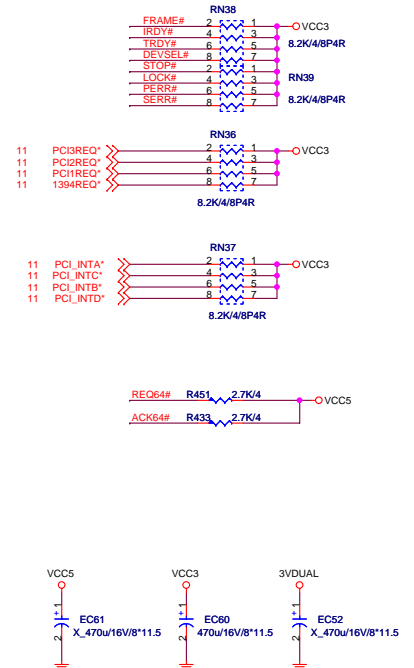
IDSEL = AD23  
MASTER = PCI2REQ\*  
PCI2GNT\*  
PCI1ROUTE=B,C,D,A

IDSEL = AD24  
MASTER = PCI3REQ\*  
PCI3GNT\*  
PCI1ROUTE=C

Medion BLUE PCI SLOT

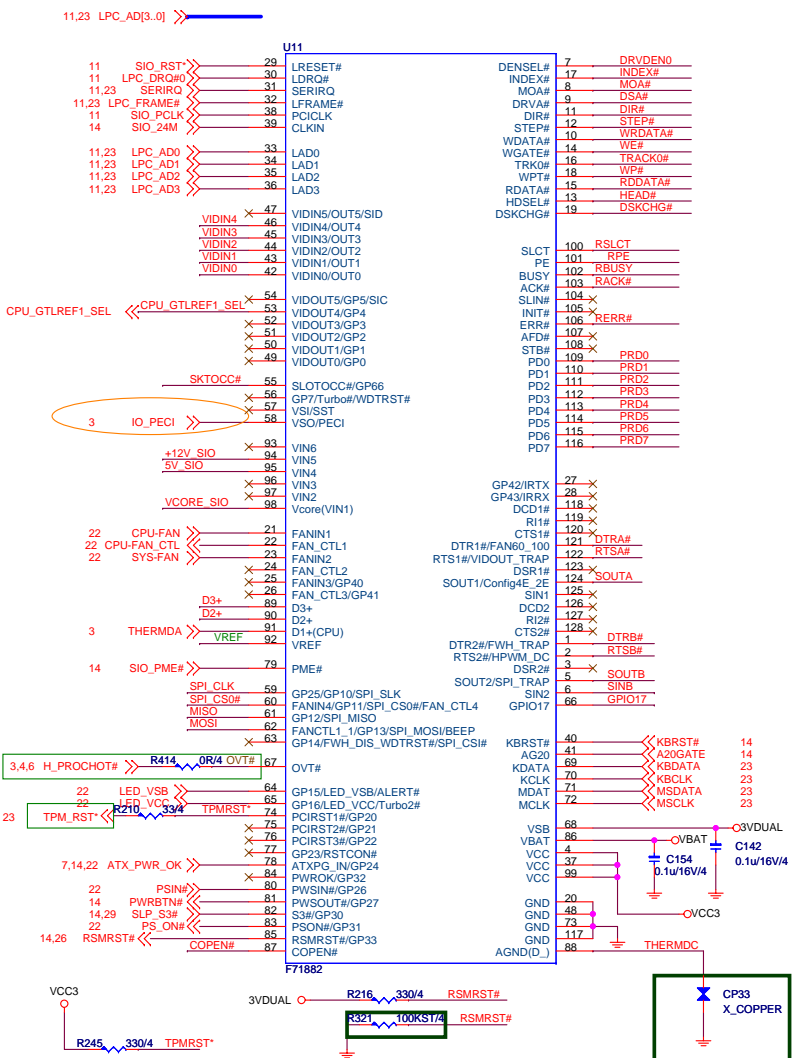


# PCI PULL-UP / DOWN RESISTORS

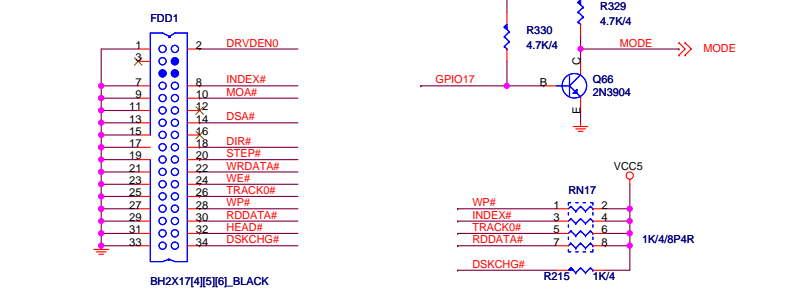


Super I/O

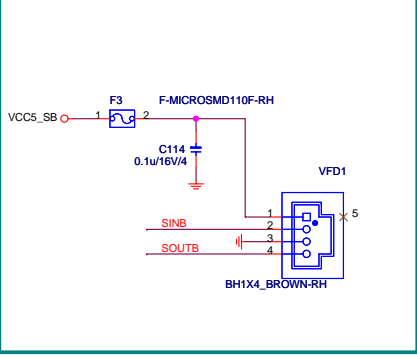
LPC SUPER I/O F71882



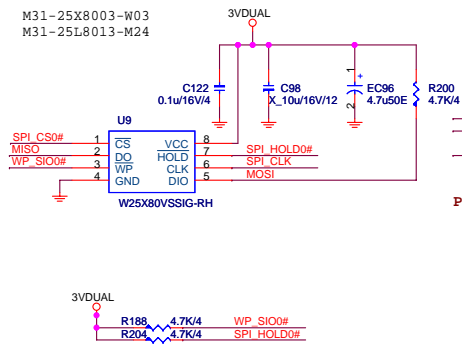
FLOPPY CONN BOLCK



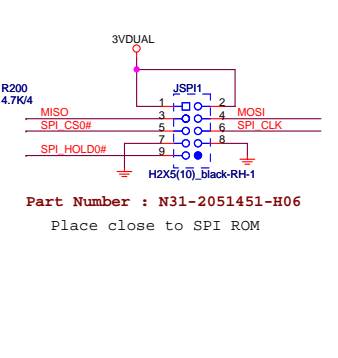
Medion VFD Pin header



SPI 8M FLASH ROM

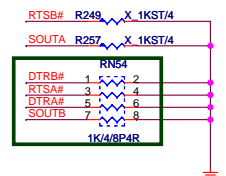


SPI DEBUG PORT



Part Number : N31-2051451-H06  
Place close to SPI ROM

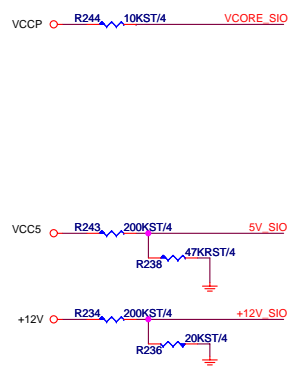
Strapping



	Don't STUFF	STUFF
RTSB#	PWM FAN	LINEAR FAN
RTSA#	PIN49-54=VID_OUT	PIN49-54=GPIO
SOUTA	PIN42-47=VIDIN	PIN42-47=VIDIN/OUT
DTRB#, SOUTB	4E	2E
DTRA#	SPI_DISABLE	SPI_ENABLE
	FAN START DUTY 60%	FAN START DUTY 100%

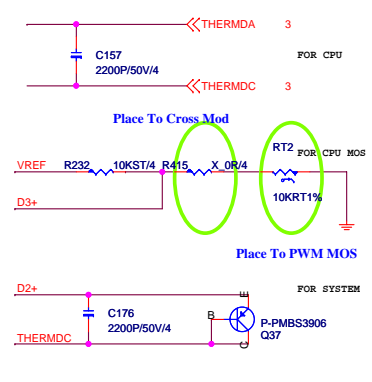
VOLTAGE SENSING(H/W Monitor).

The best voltage input level is about 1V.



Temperature Sensing

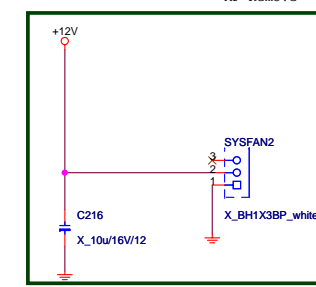
DIODE SENSING CIRCUIT



## Intel Front Panel



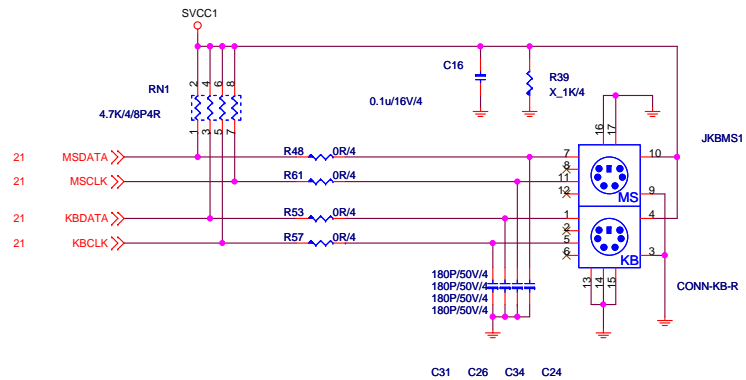
Reserve for NB\_FAN, Near MCP73  
MP Remove



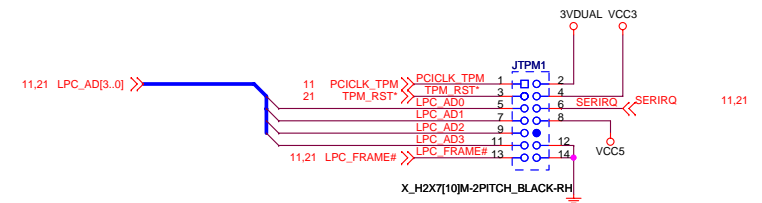
MS-7366

Size Custom	Document Description <b>ATX/Front Panel/FAN</b>	Rev 2.
Date: Tuesday, October 30, 2007		Sheet 22 of 38

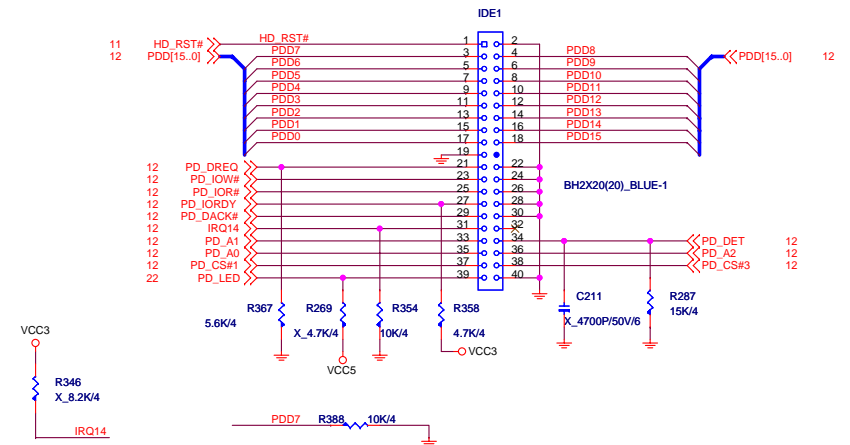
## PS2 KEYBOARD & MOUSE CONNECTOR



### JLPC port for TPM



## PRIMARY IDE BLOCK



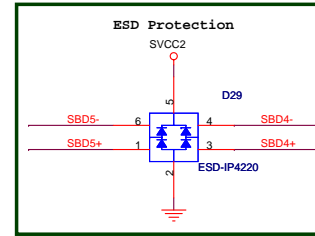
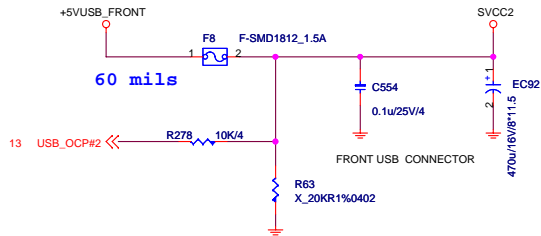
**MICRO-STAR INT'L CO.,LTD**

**MS-7366**

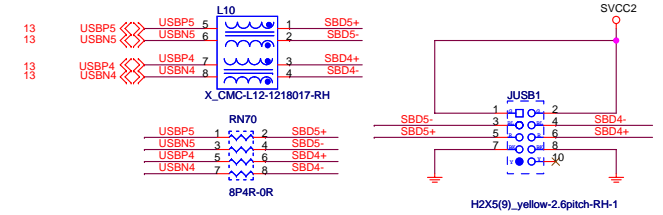
Size Custom	Document Description <b>KB/COM1/IDE/FAN</b>	Rev 2.1
Date: Tuesday, October 30, 2007		Sheet 23 of 38

# FRONT PANEL USB CONNECTOR

## POWER CIRCUIT FOR USB PORT 4,5

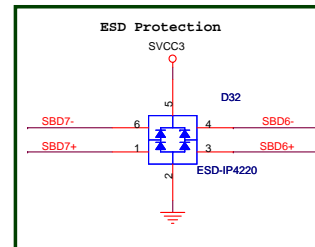
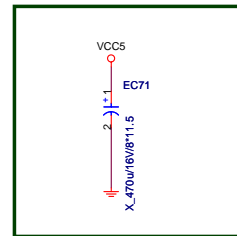
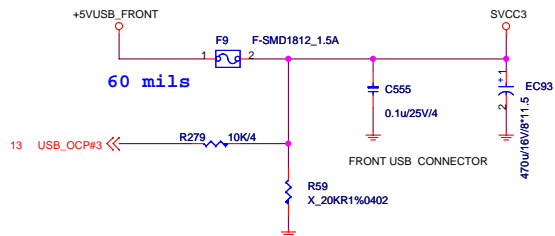


## FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

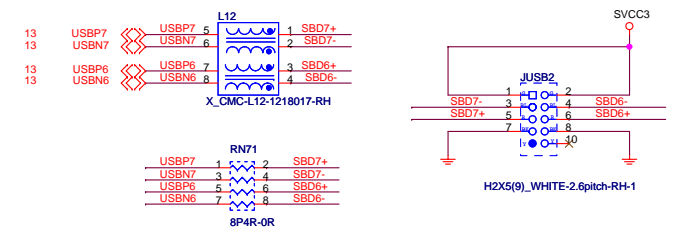


NEAR USB CONNECTOR  
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

## POWER CIRCUIT FOR USB PORT 6,7



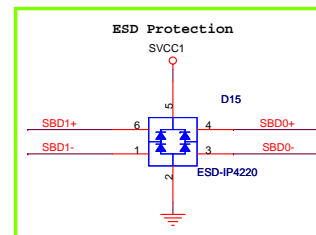
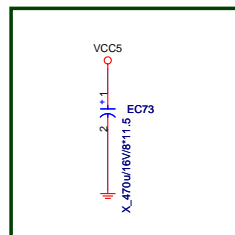
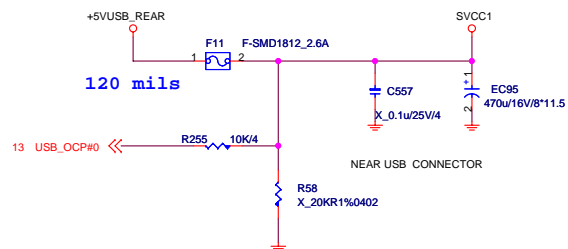
## FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



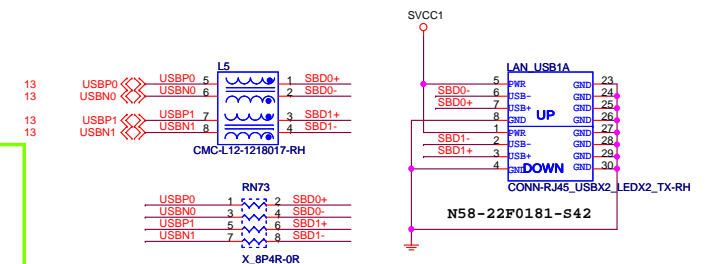


# REAR PANEL USB CONNECTOR

## POWER CIRCUIT FOR USB PORT 0,1,2,3



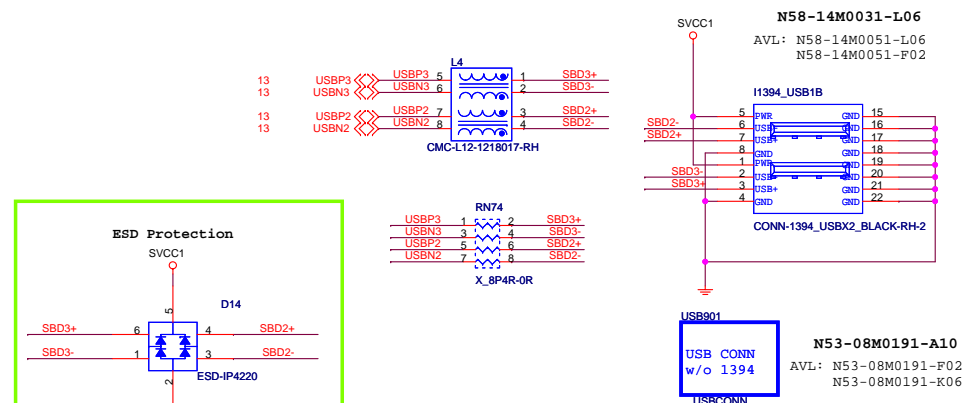
## REAR PANEL USB CONNECTOR FOR USB PORT 0,1



### NEAR USB CONNECTOR

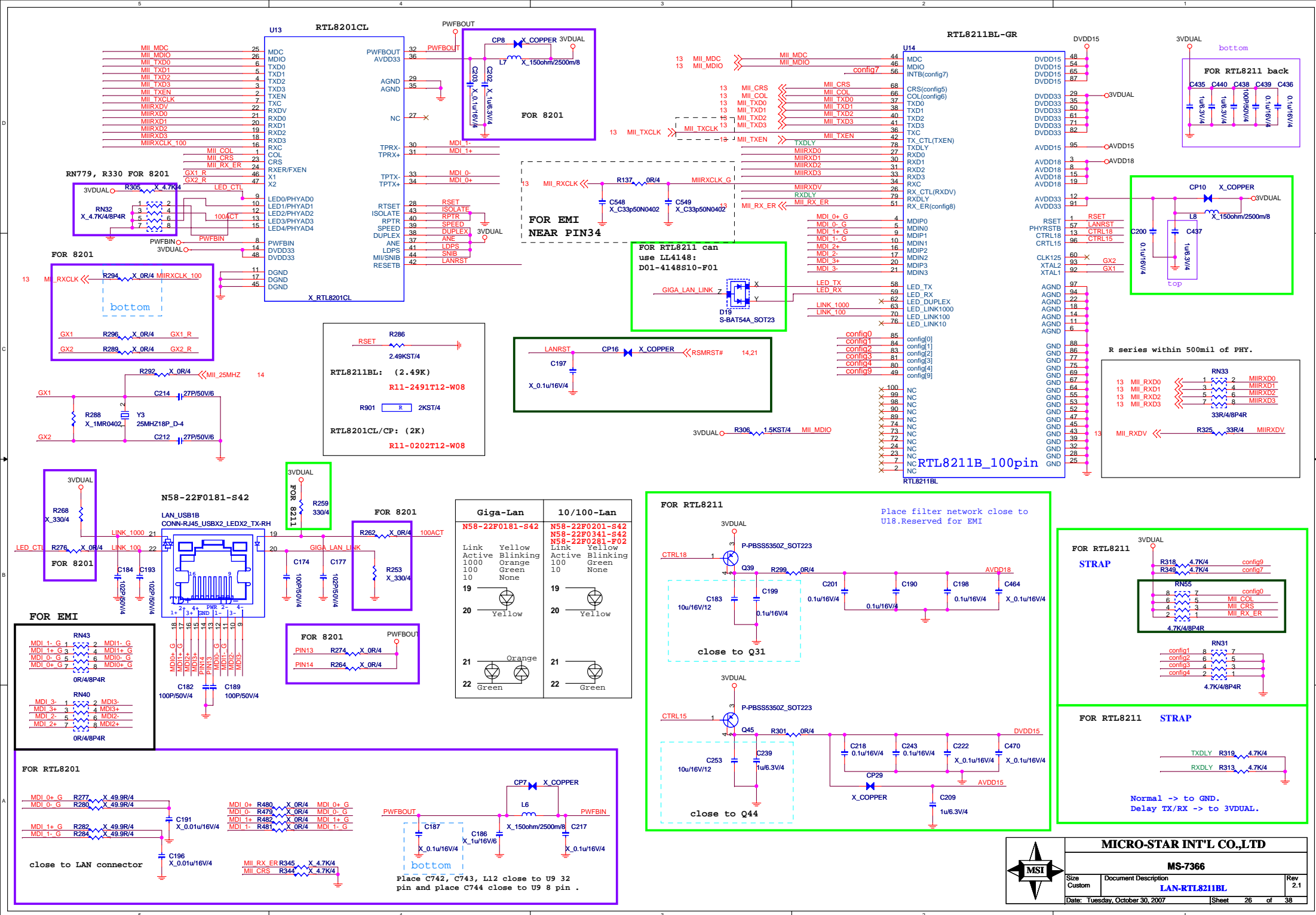
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

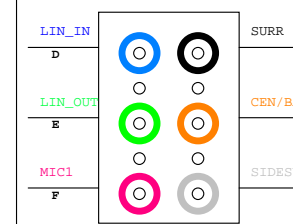
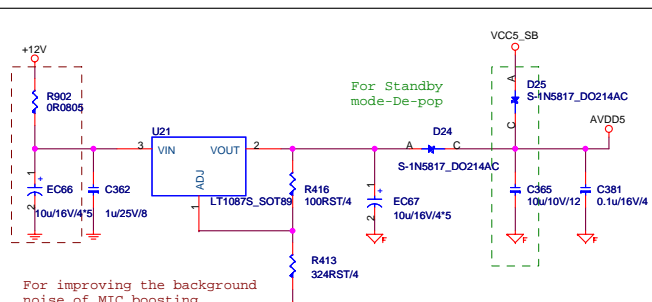
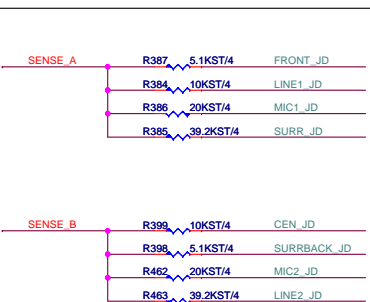
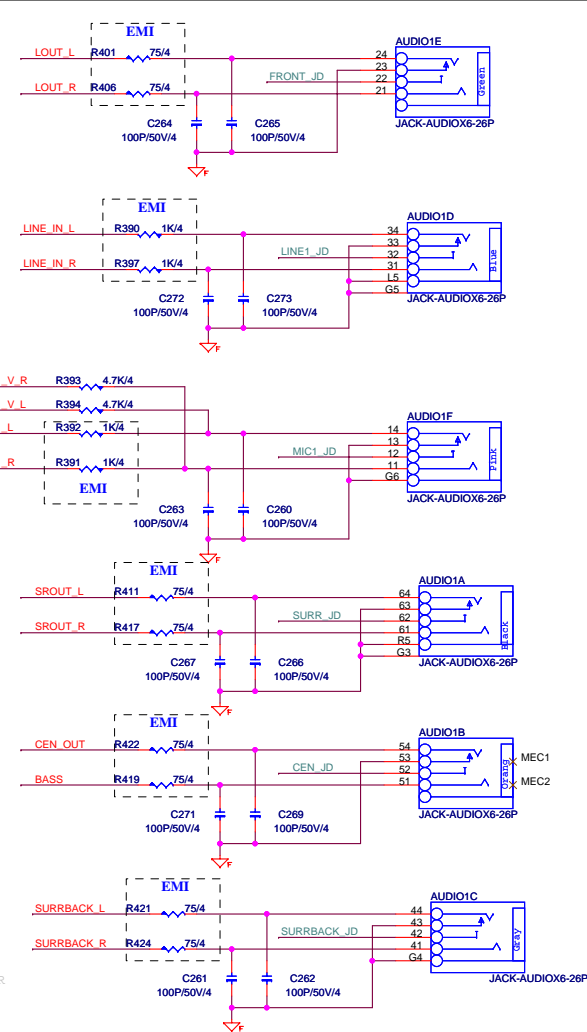
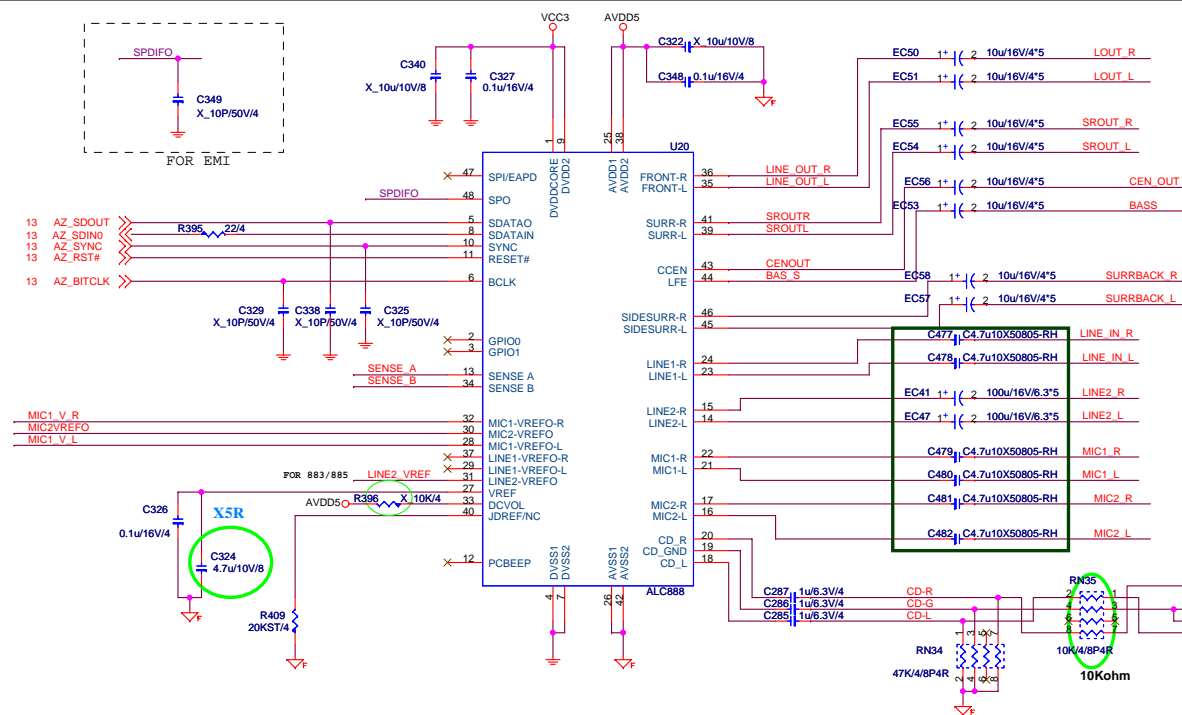
## REAR PANEL USB CONNECTOR FOR USB PORT 2,3

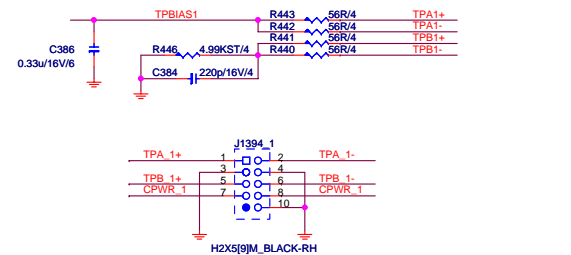
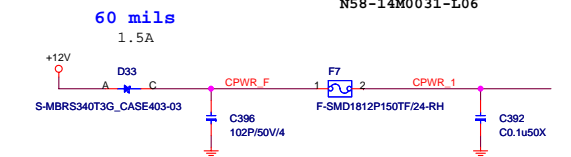
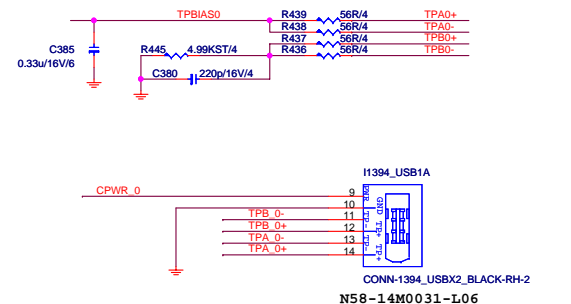
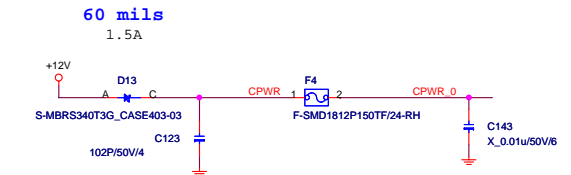
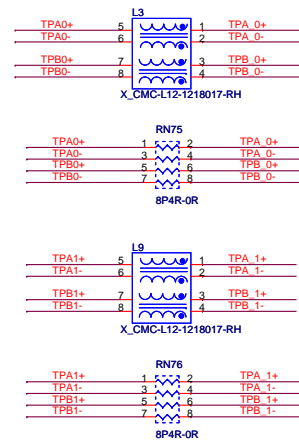
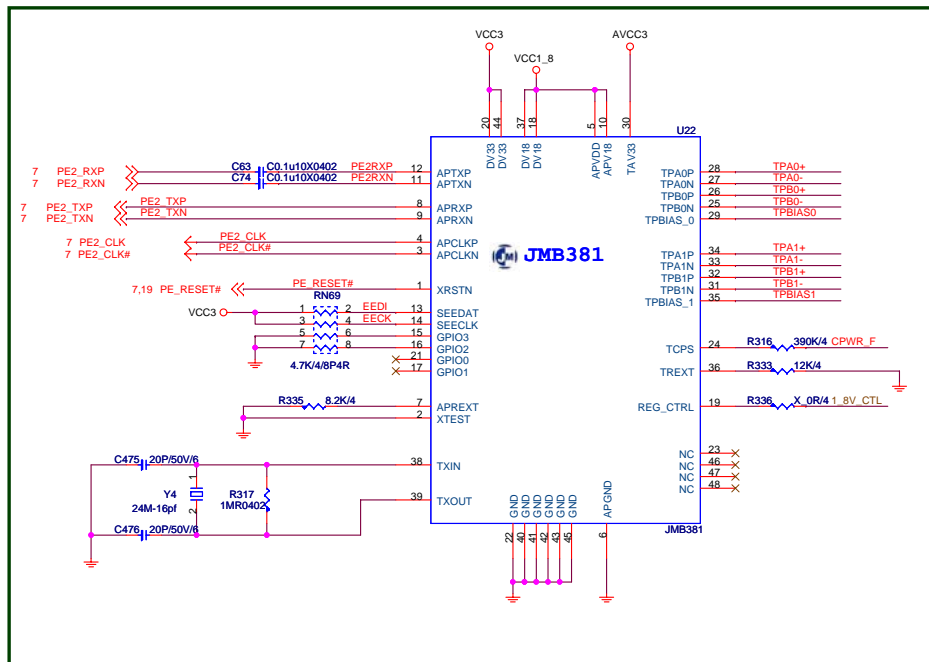


### NEAR USB CONNECTOR

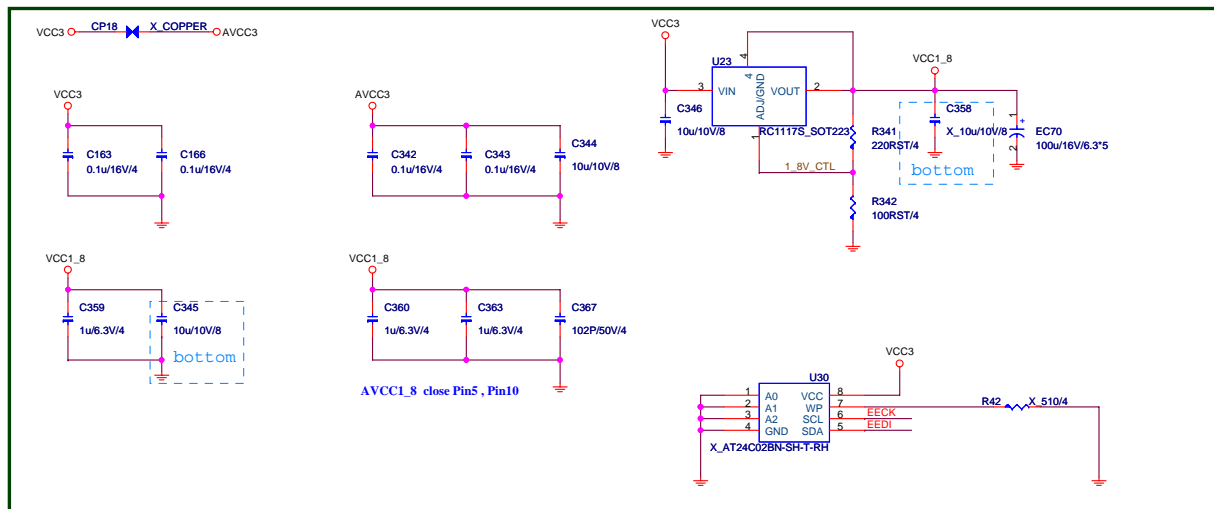
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22



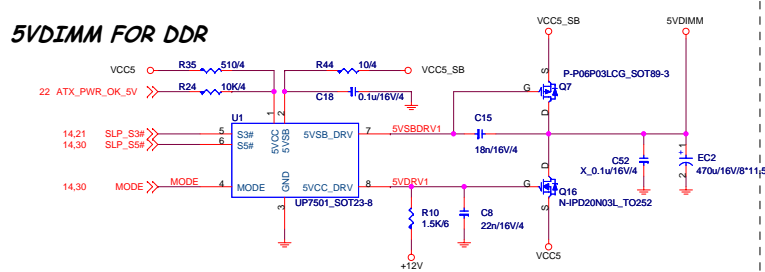




For Intel 1394 pinheader



## 5VDIMM FOR DDR

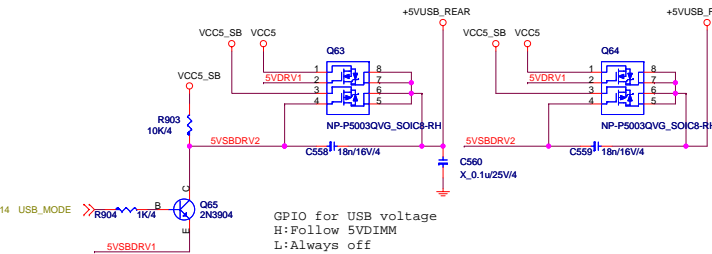


### 5VSB FOR Front USB

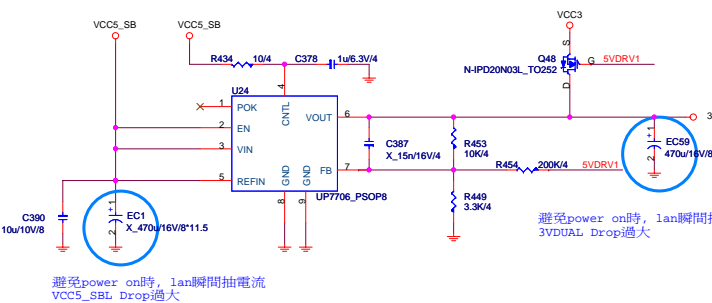
```
GPIO,Default=L
H:Support S0/S3/S5
L:Support S0/S3
```

The Dual\_CTRL must used  
default "Output- Low"

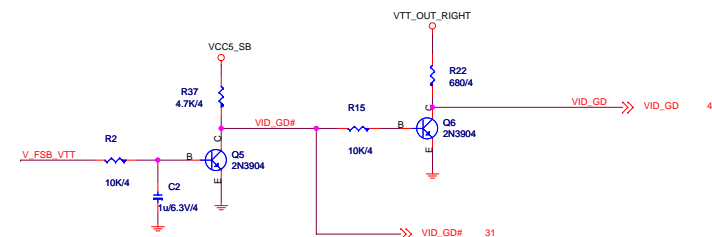
## 5VSB FOR Rear USB



## 3VDUAL, 1.7A



VID\_GD# to PWM and VID\_GD for VRM10 power sequence.



	S0	S3	S4			S5		
DUAL_CTRL	X	X	0	1	1	0	1	1
5VSBDRV1	1	0	1	0	0	1	0	0
5VDRV1	1	0	0	0	0	0	0	0
5VSBDRV2	X	0	1	0	0	1	0	0
USB_MODE	X	1	X	1	0	X	1	0
5VDIMM	Y	Y	N	Y	Y	N	Y	Y
USB power	Y	Y	N	Y	N	N	Y	N

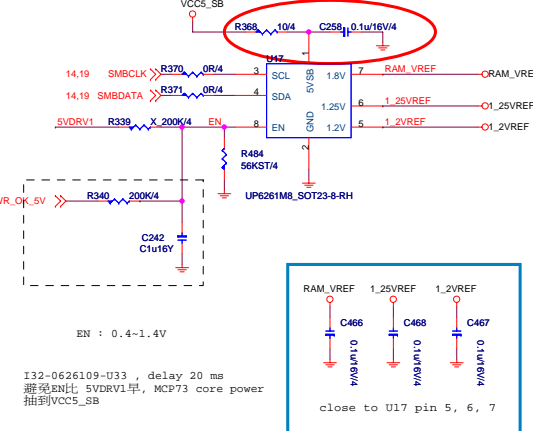
DUAL\_CTRL可控制S4/S5，USB是否要有電  
USB\_MODE控制S4，S5一種要有電一種不要有電的狀態

### Reference Voltage

up6261: High Precision Voltage Console

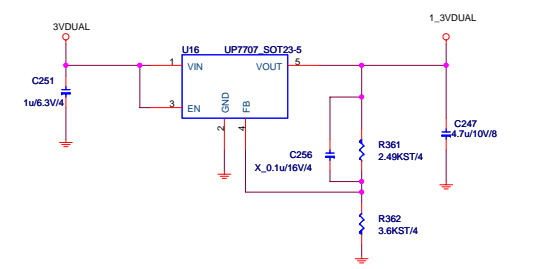
ONLY OVER DDR Voltage to 2V

VCC5\_SB to UP6261 pin1 path keep the same.



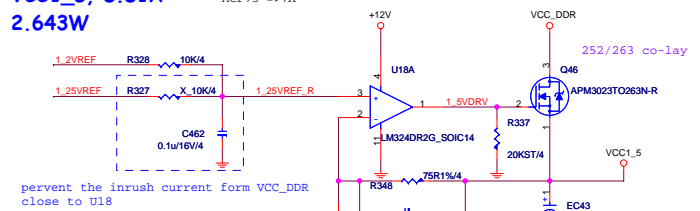
1\_3VDUAL, 25mA

up7707: 600mA Low Dropout Linear Regulator


$$V_{out} = 0.8 * (R1 + R2) / R1$$

VCC1\_5, 8.81A  
2.643W

```
H_VCCPLL=>100mA
MCP73 =>7A
```



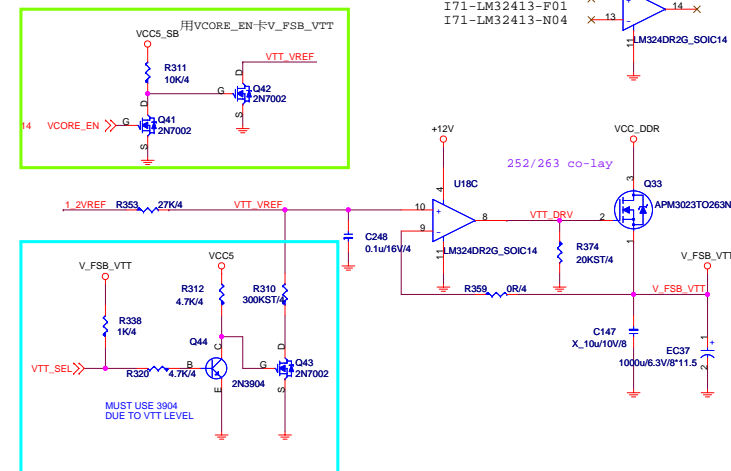
pervert the inrush current form V  
close to U18

	<b>VREF</b>	<b>1_2VREF</b>	<b>1_25VREF</b>
<b>R356</b>	<b>300R1%/4</b>	<b>100RST/4</b>	
	R11-0301T12-W08	R11-0101T12-W08	
<b>R348</b>	<b>75R1%/4</b>	<b>20RST/4</b>	
	R11-0750T12-W08	R11-0200T12-W08	

VCC1\_3, 8.81A  
1.3215W

	VREF	1_2VREF 240R1%0402	1_25VREF 249RST/4
R363		R11-0241T12-W08	R11-2490T12-W08
R369		20RST/4 R11-0200T12-W08	20RST/4 R11-0200T12-W08

FSB\_VTT, 6.1A  
3.66W



VTT_SEL = L	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H	V_FSB_VTT=1.2V	For normal processors.



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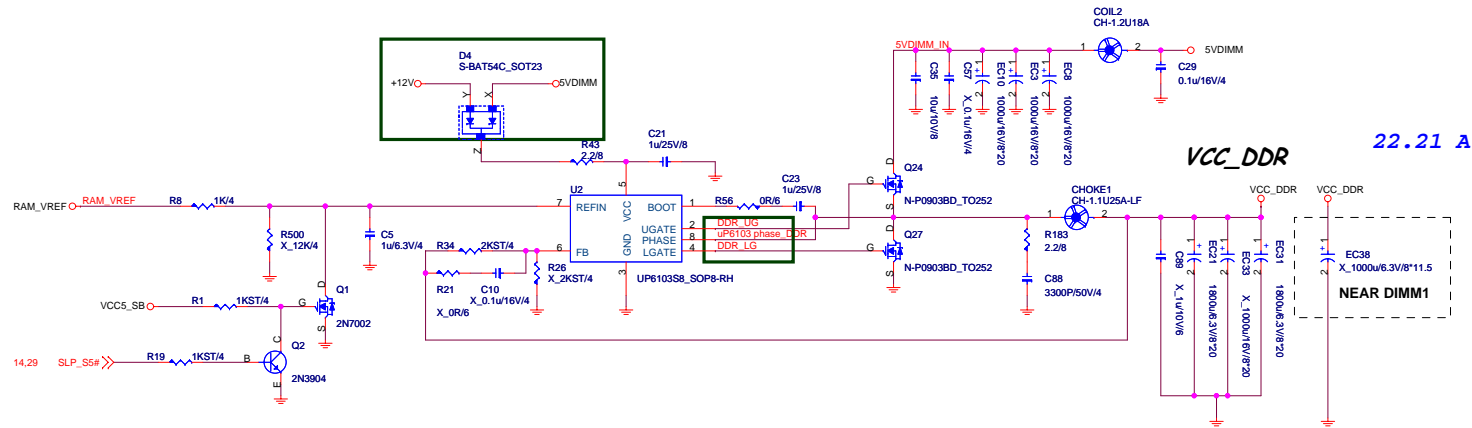
MS-7366

Size Custom	Document Description <b>ACPI Controller UPI</b>
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Rev	2.1
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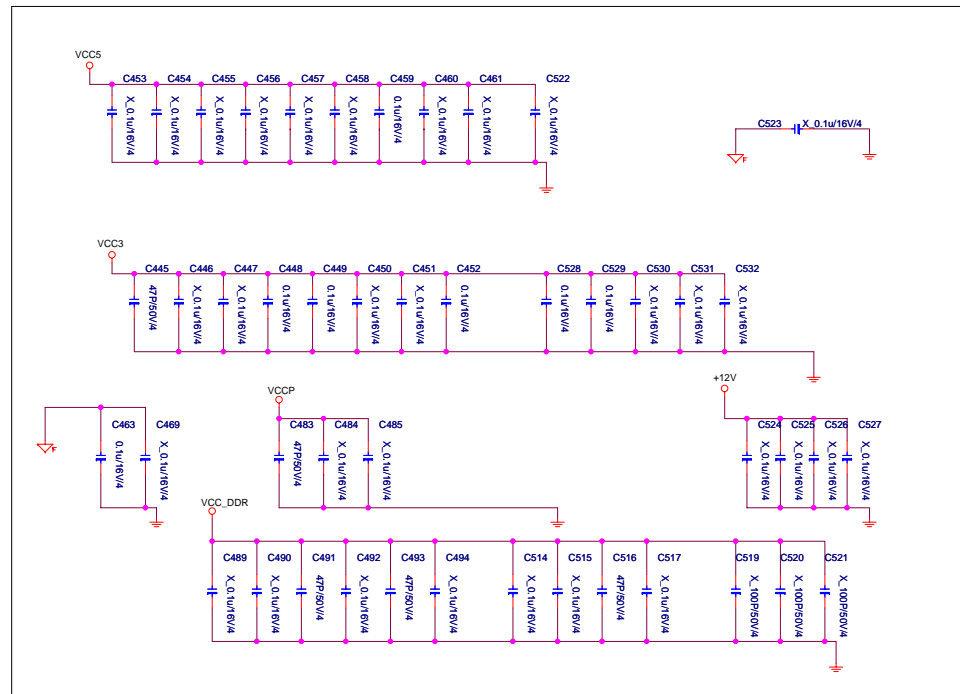
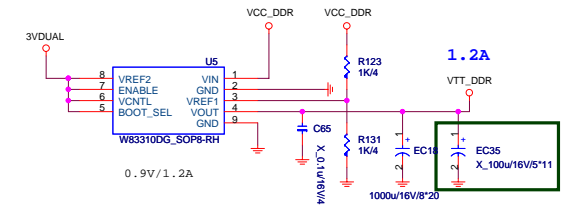
## DDR II 1.8V POWER

$$I_{ripple} = 22.21 \times 0.6 \times 0.8 / 1 = 10.66A$$

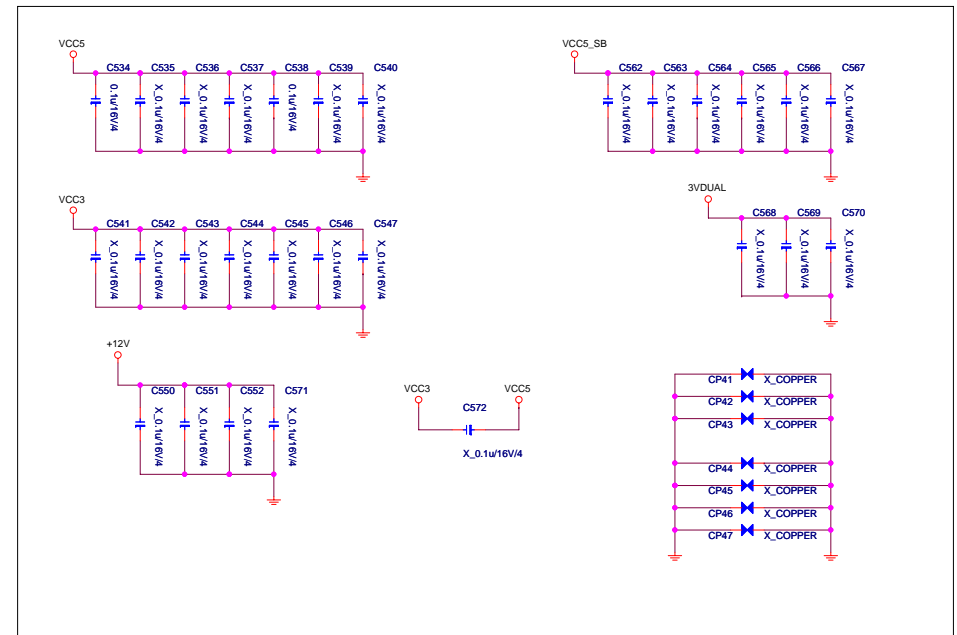
$$2.35 \times 3 \times 1.7 = 11.985A > 10.08A$$


### DDR VTT Power

To CPU Copper trace width > 200mils



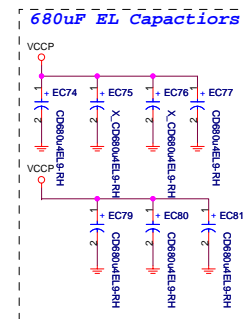
FOR EMI



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Size Custom	Document Description <b>uP6103/VT/REGULATOR</b>	Rev 2.1
Date: Tuesday, October 30, 2007		Sheet 30 of 38



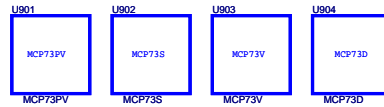
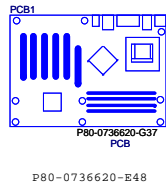
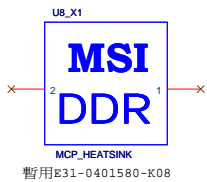
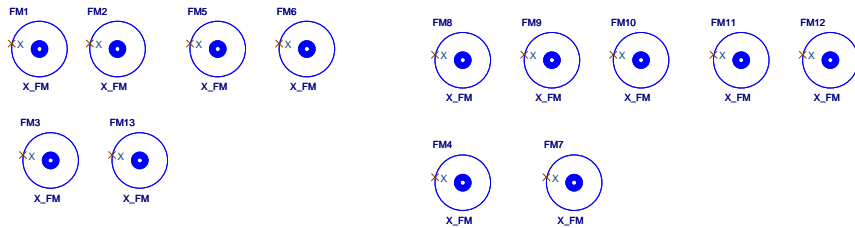


Table 1-4. Comparison of Different MCP73 Models

Features	MCP73D	MCP73PV	MCP730	MCP73S	MCP73V
IGPU	No	DX9 SM3.0	DX9 SM3.0	DX9 SM3.0	DX9 SM3.0
Display Interface	N/A	HDMI, DVI, RGB, sDVO	DVI, RGB, sDVO	DVI, RGB, sDVO	RGB
Integrated HDCP	N/A	Yes	Yes	Yes	No
FSB	1333	1333	1333	1066	1066
Memory	DDR2-667 64-bit	DDR2-667 64-bit	DDR2-667 64-bit	DDR2-667 64-bit	DDR2-667 64-bit
PCI Express	1 x16, 2 x1	1 x16, 2 x1	1 x16, 2 x1	1 x16, 2 x1	1 x16, 2 x1
USB Ports	8	10	10	10	8
Networking	10/100/1000	10/100/1000	10/100/1000	10/100/1000	10/100
SATA II Ports	4	4	4	4	4
RAID	0, 1	0, 1, 0+1, 5	0, 1, 0+1, 5	0, 1, 0+1, 5	0, 1
PATA-133	Two devices	Two devices	Two devices	Two devices	Two devices
iGPU Dev-ID	N/A	0x7E0	0x7E1	0x7E2	0x7E3
Marketing Brand Name	NVIDIA nForce 630i	NVIDIA nForce 630i GeForce 7050	NVIDIA nForce 630i GeForce 7050	NVIDIA nForce 630i GeForce 7025	NVIDIA nForce 610i GeForce 7025

### Optics Orientation Holes



### Mounting Holes

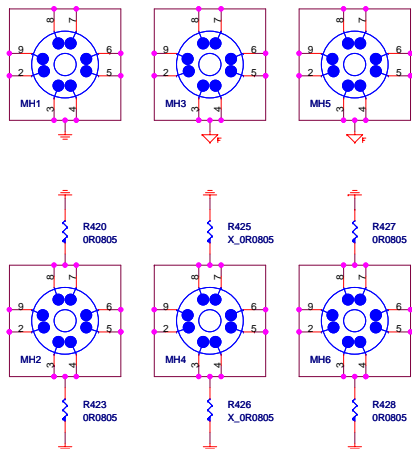


Table 1. MCP73 SKU Definition

Features	MCP73PV	MCP73S	MCP73V
FSB	1333	1333	1066
Memory	DDR2-800 64 bit	DDR2-667 64 bit	DDR2-667 64 bit
Display	HDMI, DVI, RGB, sDVO	DVI, RGB, sDVO	RGB
Integrated HDCP	Yes	Yes	No
Integrated Networking	10/100/1000	10/100/1000	10/100
Vista Premium	Yes	Yes	Yes
PCI-E	1 x16, 2 x1	1 x16, 2 x1	1 x16, 2 x1
USB Ports	10	10	8
SATA II Ports	4	4	4
RAID	0,1,0+1,5	0,1,0+1,5	0, 1
PATA Drives	2	2	2

### Simulation

